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Preliminary

IH MCU.

§ General Description:

IH MCU is an easy-used 4-bit CPU base microcontroller. It contains 4K-word ROM、128-nibble RAM、timer/Counter、interrupt service 、IO control hardware and special feature for IH applications.

§ Features:

1. Tontek RISC 4-bit CPU core
2. Total 24 crucial instructions and two addressing mode
3. Most instructions need 1 word and 1 machine cycle(2 system clocks) except read table instruction(RTB)
4. advance CMOS process
5. Working memory with 4K*16 program ROM and 128*4 SRAM
6. 4-level stacks
7. Operating voltage: 4.5V~5.5V
8. System operating frequency: (at VDD=5V)
   . High speed system oscillator (OSCH):
   - Built-in RC oscillator: 4MHz(typical at 5V)

   .Low speed peripheral oscillator (OSCL):
   - Built-in RC oscillator: 16KHz(typical)
   - RTC 32K oscillator come from OSCH
9. Offer 6~16 general programmable I/O or input pins
   - Built-in key wake-up feature enable by software setting
   - Providing external interrupt inputs and Timer clock inputs
   - Offering internal signal outputs, like buzzer(PFD)
10. One 8-bit auto-reload timer/counter & one time base counter
    - 4 timer clock sources(internal & external) selected by software
    - Timer provides the PFD feature for Buzzer output driver
    - Time base offers 2 various period interrupt request
11. MCU system protection and power saving controlled mode:
    - Built-in watch dog timer (WDT) circuit
    - Providing high system operating speed.

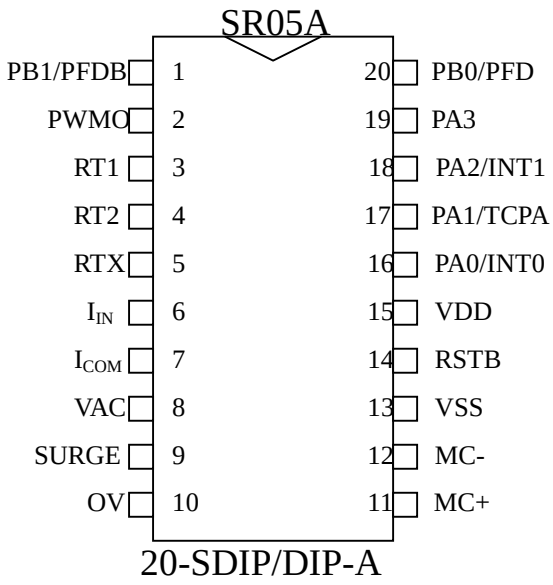
- Built-in low voltage reset (LVR) function

12. Induction Heating special peripheral device
    - Power measurement and production
    - Thermal measurement and production
    - IGBT driver and production
13. Provides 8 interrupt sources
    - External: INT shared with IO pad
    - Internal: Timer/counter A, peripheral device & Time base timer
14. Provide package types
    - DIP/SOP/SSOP 20/24/28/32 pins

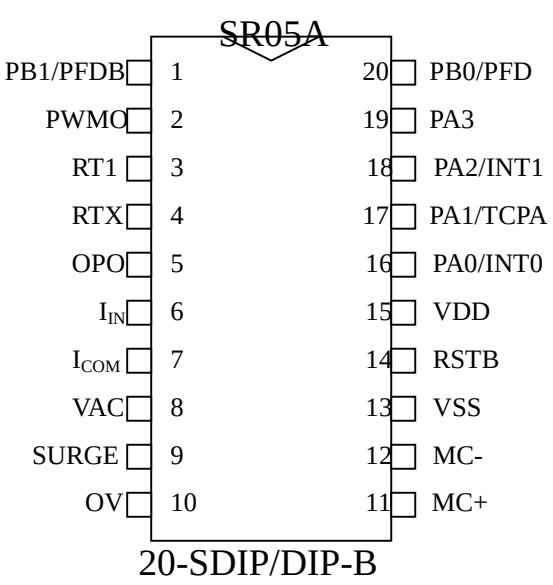
§ Applications:

1. Household electric appliances (IH cooker)
2. Consumer products
3. Measurement controller

§ Package type:

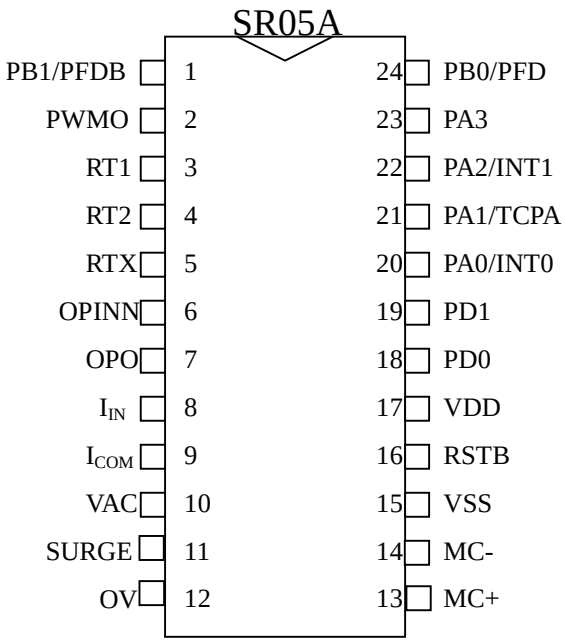


20-SDIP/DIP-A



20-SDIP/DIP-B

Preliminary



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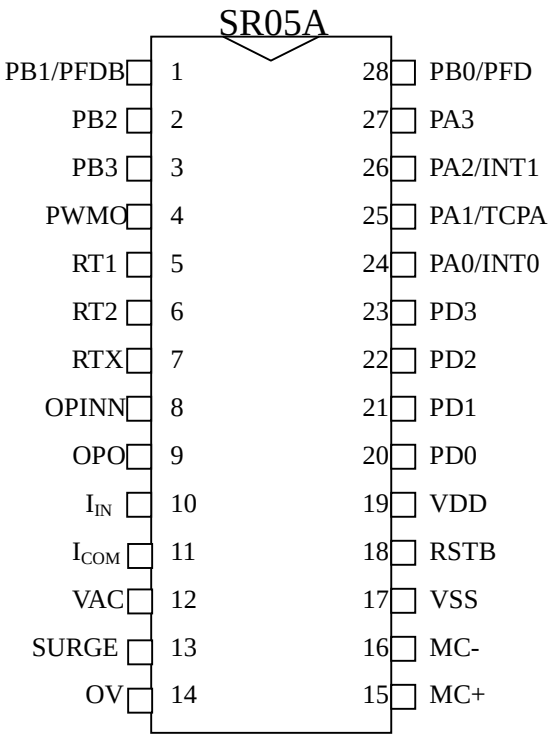

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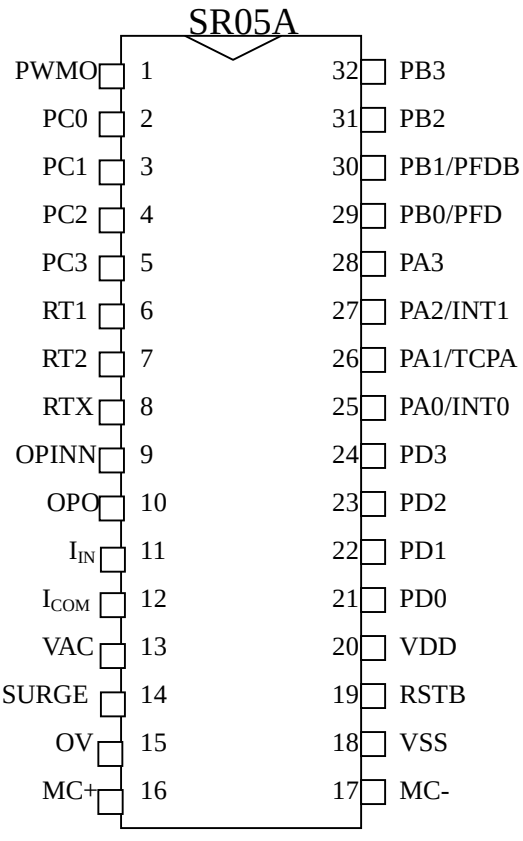

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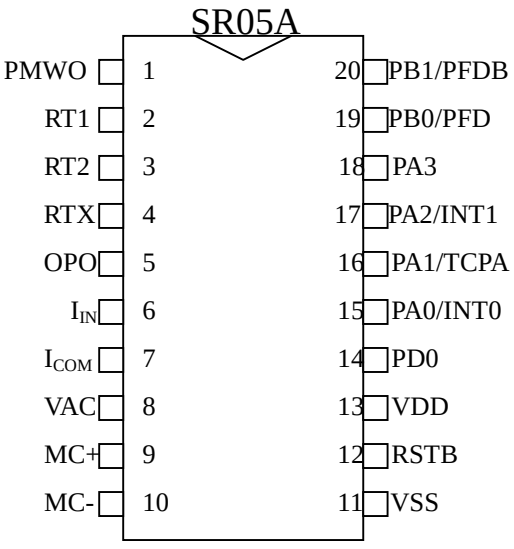
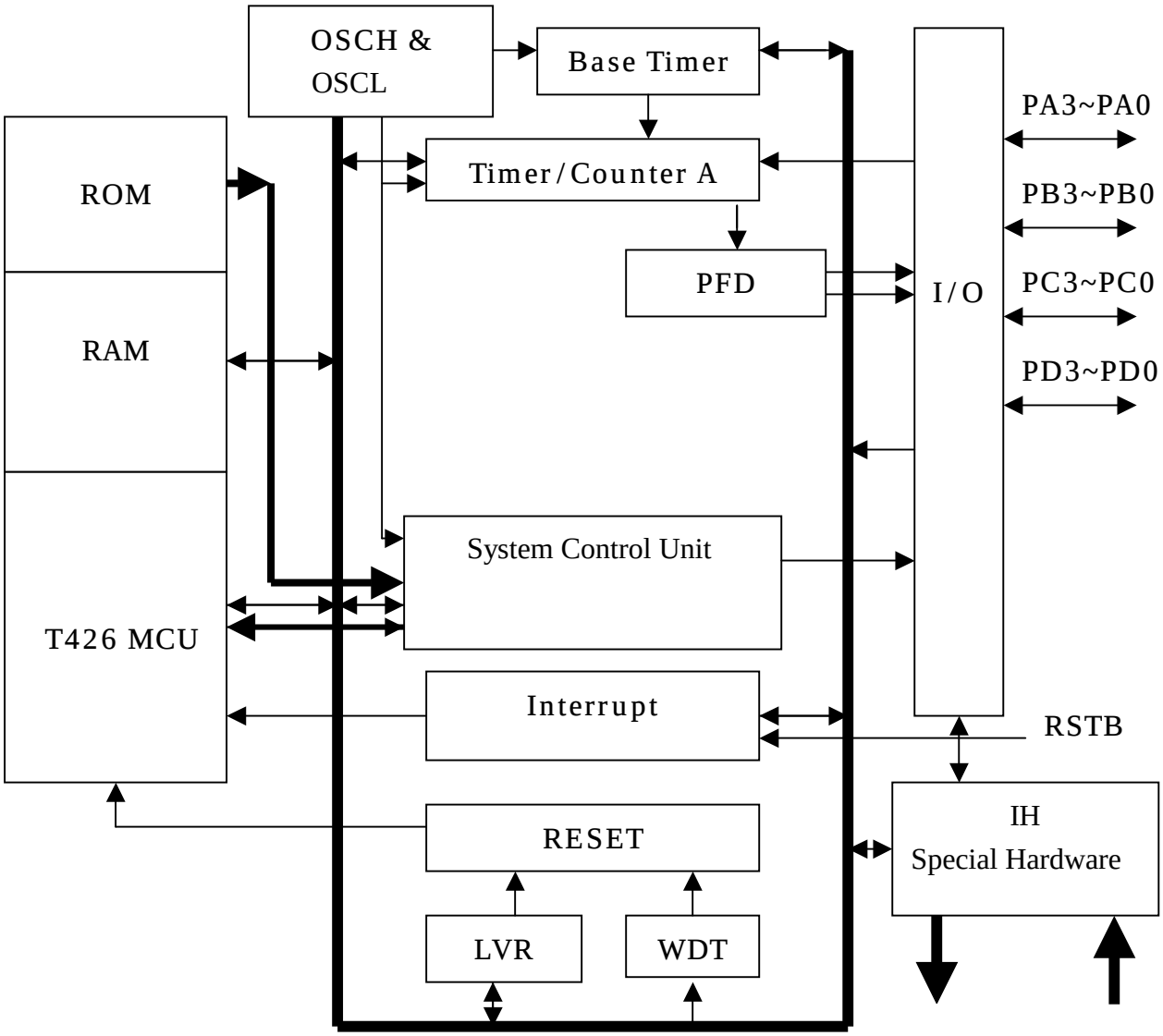


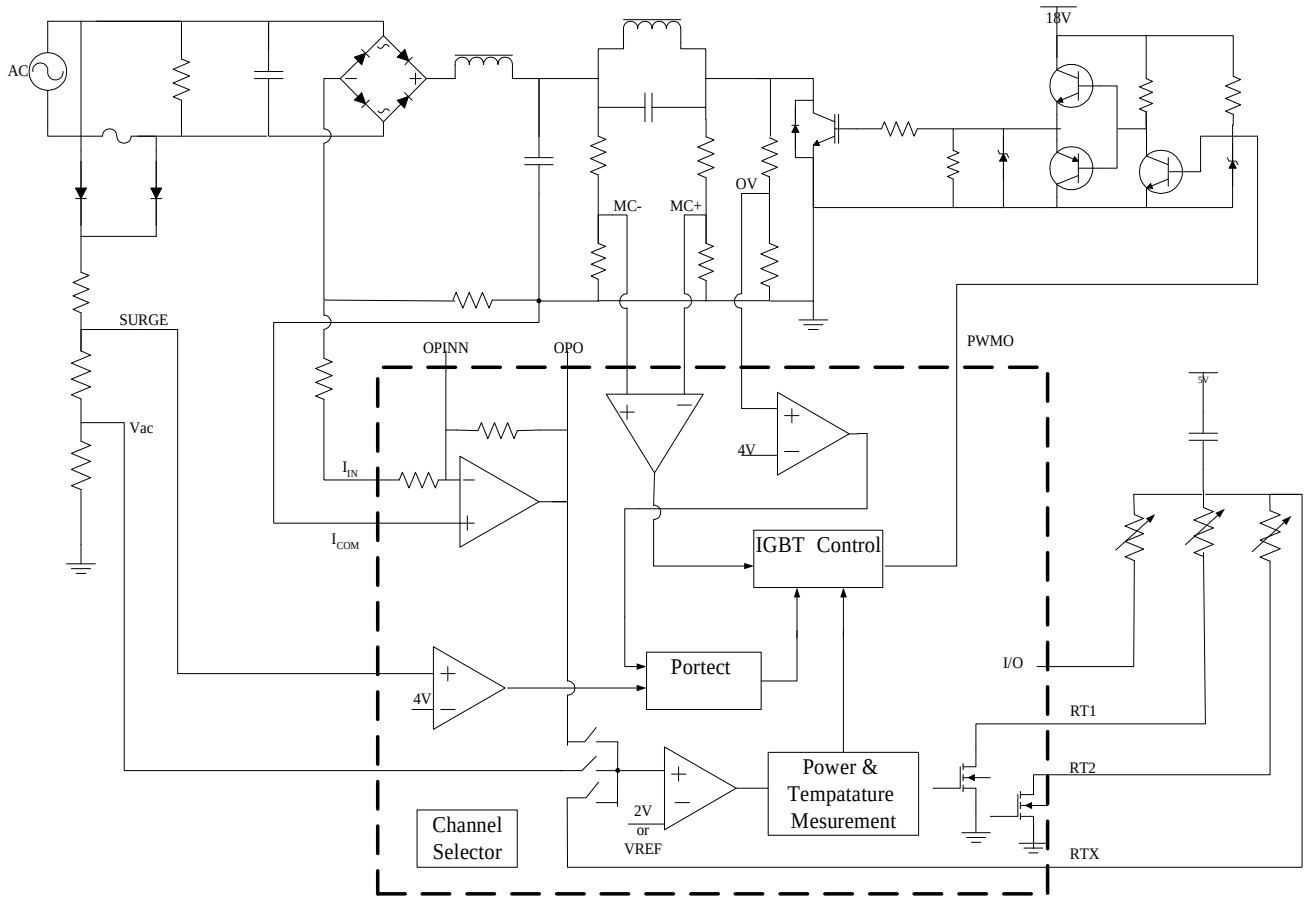
20-SDIP/DIP-C

§ Block Diagram:

² System Block



2 IH Block



§ Pin Description:

Pin Name	I/O	Pin Description
RSTB/VPP	I	External reset input, active low 50kΩ pull-up(5v)
V_{DD}	Power	Positive power supply
PA0(INT)	IO	I/O port with external interrupt input (PA0). PA1 used as clock inputs of timer/counter A
PA1(TCPA)	IO	
PA2	IO	
PA3	IO	
PB0(PFD)	IO	I/O port with internal signal output
PB1(PFDB)	IO	
PB2	IO	
PB3	IO	
V_{SS}	Power	Negative power supply, ground
PC0~PC3	IO	IO port
PD0~PD3	IO	IO port
MC+	I	PWM synchronic positive input
MC-	I	PWM synchronic negative input
Vac	I	AC power over range
OV	I	IGBT overshot voltage detector input
I_{IN}	I	Power current input
OPINN	I	OP negative input
OPO	O	OP Amp output
I_{COM}	I	OP positive input
RTX	I	Common input
RT1	O	RT1 enable output
RT2	O	RT2 enable output
SURGE	I	AC line surge input
PWMO	O	PWM output NMOS open drain

§ IO Cell type Description:

Pin Name	I/O Type	Description
PA0~PA2	Figure IO-A	STD IO with external input
PB0~PB1	Figure IO-B	STD IO with internal output
PA3,PB2~PB3	Figure IO-C	STD IO
PC0~PC3	Figure IO-A	STD IO with external input
PD0~PD3	Figure IO-A	STD IO with external input

§ Absolute Maximum ratings:

ITEM	SYMBOL	RATING	UNIT
Operating Temperature	Top	-20℃ ~ +70℃	℃
Storage Temperature	Tst	-50℃ ~ +125℃	℃
Supply Voltage	VDD	VSS-0.3 ~VSS+6.0	V
OTP Supply Voltage	VPP	VSS-0.3 ~ VSS+12.5	V
Input Voltage	Vin	VSS -0.3 to VDD+0.3	V
Human Body Mode	ESD	>5	KV
Note: VSS symbolizes for system ground			

§ DC Characteristics: (Test condition at room temperature=25°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Operating Voltage	VDD	F_{OSCH}=4MHz (LVR ON)	4.0 4.0	- -	5.5 5.5	V
Operating Current (Normal Mode, CPU working, I/O no load)	I_{nd1}	VDD=5.0V, no load,	-	1.5	2.0	mA
Input Ports	V_{IL}	Input Low Voltage	0	-	0.2	VDD
Input Ports	V_{IH}	Input High Voltage	0.8	-	1.0	VDD
RESET & INT	V_{IL}	Input Low Voltage	0	-	0.3	VDD
RESET & INT	V_{IH}	Input High Voltage	0.7	-	1.0	VDD

Output port Sink Current	I_{OL}	VDD=5.0V, V_{OL}=0.6V	-	8	-	mA
Output Port Source Current	I_{OH}	VDD=5V, V_{OH}=VDD-0.7V	-	-4	-	mA
I/O Port Pull-High Resistor	R_{PH}	VDD=5.0V	100	150	200	KΩ
RESET Pull-High Resistor	R_{PH}	VDD=5.0V	30	50	80	KΩ
Low Voltage Reset (LVR)	V_{LVR1}	For AC application	2.4	3.2	4.0	V
Oscillator Start up voltage	$\mathbf{V_{ST}}$	F_{OSC}=4MHz	2.4	-	-	V

§ AC Characteristics:

Parameter	Test Condition		Min	Typ.	Max	Unit
External Reset	Low active pulse width $\mathbf{t_{RES}}$		2	-	-	CPU clock
Interrupt input	Low active pulse width $\mathbf{t_{INT}}$		2	-	-	
Wake up input	Low active pulse width $\mathbf{t_{wkup}}$, Application de-bounce should be manipulated by user' software		2	-	-	OSCL
System Oscillator Frequency	F_{OSCH}	VDD=5.0V	-	4M	-	Hz
System Stable Time after Power up	After power up, the system needs to initialize the configured state and OST.		-	-	64	ms

§ Memory Map:

ROM ADDRESS	RAM ADDRESS	Function Block
000_H~FFF_H		Program ROM [4K*16]
	000_H ~ 007_H	File Registers
	008_H~$01F_H$	Peripheral registers (I)

	020_H~$09F_H$	Working RAM [128*4]
	120_H~133_H	Peripheral registers (II)

§ Interrupt Vectors:

Interrupt Vectors	Function Description
$000	hardware RESETB
$001	Hardware IRQB1

§ File registers:

Address	Symbol	R/W	Default	Description
000_H	(DP1)	R/W	-	Indirect addressing register
001_H	ACC	R/W	-	Accumulator & Read Table 1st data
002_H	TB1	R/W	-	Read Table 2nd data
003_H	TB2	R/W	-	Read Table 3rd data
004_H	TB3	R/W	-	Read Table 4th data
005_H	DPL	R/W	-	Data Pointer low nibble
006_H	DPM	R/W	-	Data Pointer middle nibble
007_H	DPH	R/W	-	Data Pointer high nibble

§ Peripheral registers: Interrupt request flag register

Address	Symbol	R/W	Default	Description
008_H	PS	R/W	----	Power saving control register
009_H	INTC0	R/W	0000	Interrupt enable control register
$00A_H$	INTF0	R/W	0000	Interrupt request flag register
$00B_H$	TBC	R/W	1111	Time base control register

$00C_H$	TCPAC	R/W	0000	TCPA Timer/counter A control register
$00D_H$	TCPAL	R/W	0000	TCPA Timer/counter A data low register
$00E_H$	TCPAH	R/W	0000	TCPA Timer/counter A data high register
$00F_H$	PAC	R/W	1111	I/O port A control register
010_H	PA	R/W	1111	I/O port A data register
011_H	PBC	R/W	1111	I/O port B control register
012_H	PB	R/W	1111	I/O port B data register
013_H	PCC	R/W	1111	I/O port C control register
014_H	PC	R/W	1111	I/O port C data register
015_H	PDC	R/W	1111	I/O port D control register
016_H	PD	R/W	1111	I/O port D data register
017_H	PSP	R/W	--00	Peripheral power saving control register
018_H	INTC1	R/W	0000	Extended interrupt enable register
019_H	INTF1	R/W	0000	Extended interrupt request flag register
$01A_H$	TCPFS	R/W	-000	TCP clock source FS pre-scale register
$01B_H$	CPACK	R	0000	CP acknowledge date register
$01E_H$	PWMDL	R/W	0000	Low nibble PWM output data
$01F_H$	PWMDH	R/W	0000	High nibble PWM output data
120_H	MESDL	R	0000	Low nibble MES output data
121_H	MESDH	R	0000	High nibble MES output data
122_H	CPSEL	R/W	-000	Comparator channel select register
123_H	TZERO	R/W	-000	Adjustable time for zero voltage register
127_H	TBCC	W	----	Time base counter clear address
129_H	PAI	R	----	Port A pad data reading address
$12A_H$	PBI	R	----	Port B pad data reading address
$12B_H$	PCI	R	----	Port C pad data reading address
$12C_H$	PDI	R	----	Port D pad data reading address
$12D_H$	MESCKSEL	R/W	-000	Measure clock selection register
$12E_H$	OPGFSEL	R/W	0000	OP Amp Gain factor selection register
130_H	RESETF	R/W	0-00	Reset flag
131_H	MRO	W	----	Mask option register write enable address

Note: a. Default means initial value after power on or reset.

b. R is “read” only, W is “write” only, R/W is both of “read” & “write”.

§ System function description:

1: System Oscillators

The high speed oscillator was built-in an RC 4MHz oscillator.

2: Peripheral Oscillators

The peripheral oscillator comes from built-in 4M RC oscillator provides 32KHZ frequency.

3: CPU clock

The CPU clock comes from system oscillator which was built-in 4M RC oscillator.

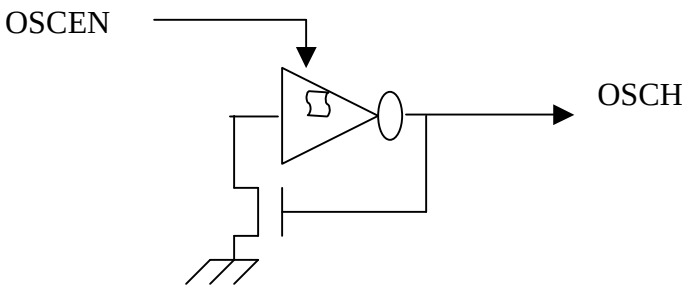


Figure: System High Speed Oscillator

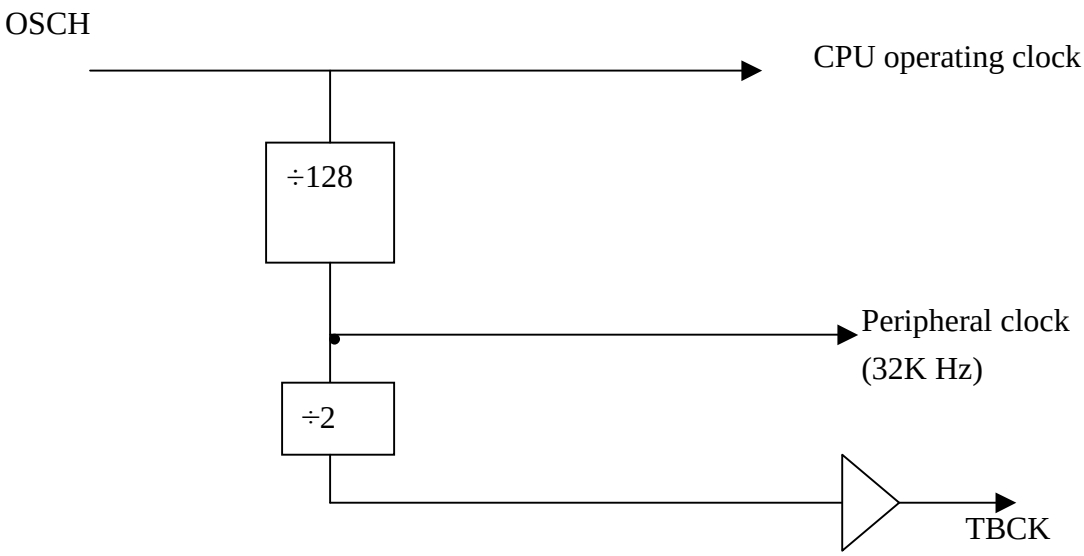


Figure: System Oscillator & CPU Clock Sources

4: Watch Dog Timer (WDT)

The clock of watch dog timer comes from time base overflow (TB1OV). User can use the time up signal to prevent a software malfunction or abnormal sequence from jumping to an unknown memory location causing a system fatal failure. Normally, if the watchdog timer time up signal active that will reset the chip. At the same time, program and hardware can be initialized and resume system under normal operation. The chip also provides clear watchdog command as the programmer writes INTF with $F data. Completely finishes the two write steps will clear the watch dog timer. User should well arrange the two command steps for avoiding the dead lock loop.

User should keep in minds that always reset WDT at main program and never clear the WDT in the interrupt routine.

The max period of WDT = (TB1OV cycle time) * 8

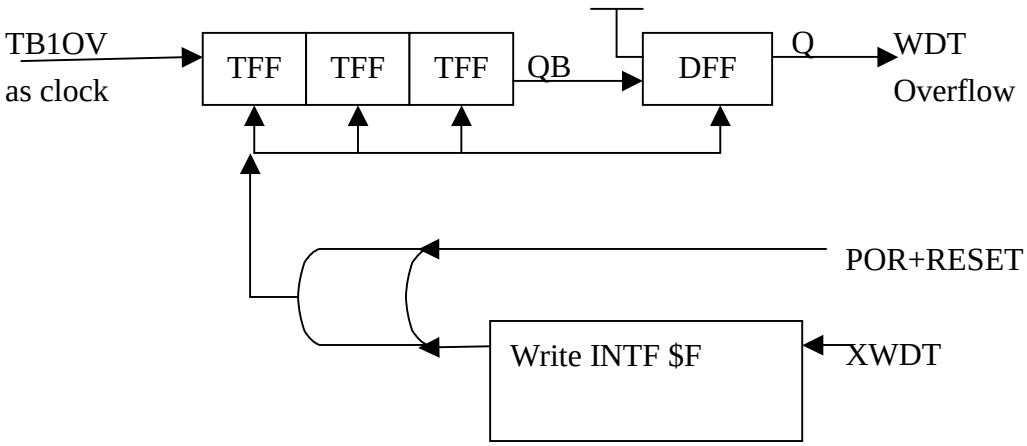


Figure: Watch Dog Timer control circuit

5: Low Voltage Reset (LVR)

The low voltage reset (LVR) forces the MCU in reset state during power failure, especially

as MCU working in AC power application, preventing from abnormal state is the key issue.

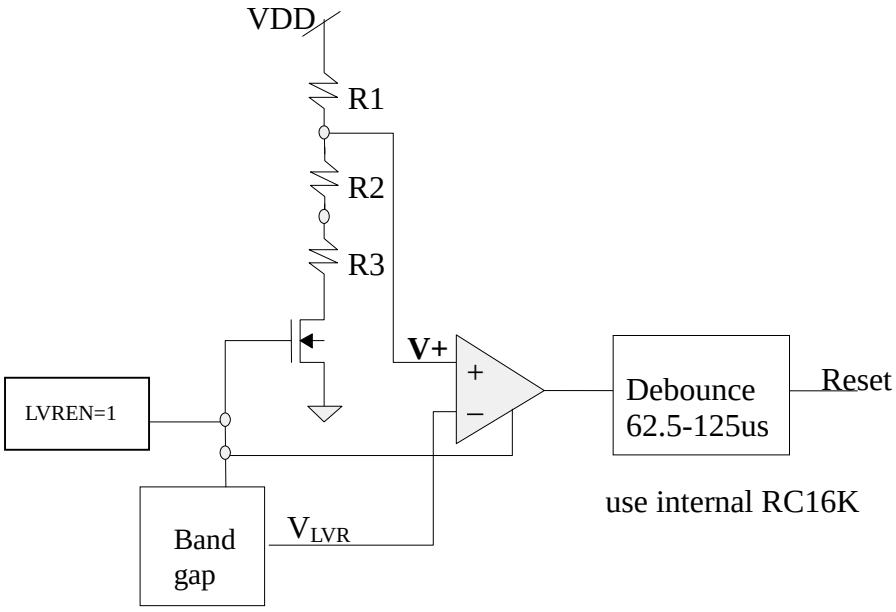


Figure: Low Voltage Reset or Low Voltage Detector

6: RESET

The chip has five kinds of reset sources: POR (power on reset), External reset, Watch dog timer reset, LVR (low voltage reset), LVNCR (low voltage reset for no clock detection).

.POR (power on reset)

The chip provides automatic reset function when the power is turned on. The VDD should be below 1.6V and its rising slope (from 0.1VDD up to o.9VDD) needs less than 10ms.

.External Reset (RSTB)

This is one kind of system resetting signal, but only forced externally. When the chip acknowledged the low level from the pin RSTB exceed 1 us, it will generate the reset procedure to reset CPU & all the peripheral back to their initial state (default values).

.Watch Dog Timer Reset

The reset signal will generate automatically when the watchdog timer runs overflow. If

the watchdog timer is cleared regularly by users' program, no watchdog reset will occur. Unless the MCU is forced into abnormal state, the software controlled procedure is disrupted and causing watch dog timer overflow, then it will generate reset signal to initializes the chip returning to normal operation.

.Low Voltage Reset (LVR)

The LVR function is used to monitor the supply voltage of MCU, it will generate a reset signal (with 62.5-100us de-bounce time) to reset the microcontroller as the VDD power falls below the default setting level V_{LVR}.

. LVNCR (low voltage reset for no clock detection)

The LVNCR is an oscillator clock detector. If OSCH clock is stopped under normal condition, then LVNCR signal with rising edge and sets the LVNCRF=1. By the way, the system reset will start the system reset procedure.

² RESETF: reset source flag register[R/W], power on value [0-00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	LVNCRF	-	LVRF	WDTF
Read/Write	R/W	-	R/W	R/W

WDTF: Watch dog timer overflow reset flag (0: no active; 1: active)

LVRF: Low voltage reset flag (0: no active; 1: active)

(The RESETF is only cleared by system reset that included POR and external reset.)

LVNCRF: OSCH clock detection circuit (0: normal; 1: abnormal)

7. Power saving control register

² PS: Power saving register[R/W] , default value [----]

PS register	Bit3	Bit2	Bit1	Bit0
Bit Name				
Read/write				

² PSP: Peripheral power saving register[R/W] , default value [--00]

PSP register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	PFDEN	PWMEN

Read/write	-	-	R/W	R/W

PWMEN: PWM enable (0: disable; 1: enable)

PFDEN: PFD & PFDB output enable (0: disable; 1: enable)

8. Interrupts

The CPU provides only 1 interrupt vector ($001H) and no priority, but can expand to multi-sources. The interrupt control registers (INTC0 and INTC1 contain the interrupt control bits to enable and disable corresponding interrupt request and the corresponding interrupt request flags in the (INTF0 and INTF1) registers. Before finishing the INT service routine, another INT request will keep waiting until program return from interrupt routine.

- INTC0: Interrupt control register [R/W], default value [0000]

INTC0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESIE	TCPAIE	TB2IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

TB1IE: Enable time base 1st interrupt. (0: disable; 1: enable)

TB2IE: Enable time base 2nd interrupt. (0: disable; 1: enable)

TCPAIE: Enable interrupt of timer/counter A. (0: disable; 1: enable)

MESIE: Enable interrupt of MES counter. (0: disable; 1: enable)

- INTF0: Interrupt request flag register [R/W], default value [0000]

INTF0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESF	TCPAF	TB2F	TB1F
Read/Write	R/W	R/W	R/W	R/W

TB1F: Time base timer 1st interrupt request flag. (0: inactive; 1: active)

TB2F: Time base 2nd interrupt request flag. (0: inactive; 1: active)

TCPAF: Timer/counter A′ interrupt request flag. (0: inactive; 1: active)

MESF: MES counter interrupt request flag. (0: inactive; 1: active)

- INTC1: Extended interrupt control register [R/W], default value [0000]

INTC1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEIE	IGBTOVIE	SYNCIE	INTIE
Read/Write	R/W	R/W	R/W	R/W

INTIE: INT external interrupt request enable. (0: disable; 1: enable)

SYNCIE: SYNC interrupt request enable. (0: disable; 1: enable)
IGBTOVIE: IGBT over voltage interrupt enable. (0: disable; 1: enable)
SURGEIE: Surge interrupt enable. (0: disable; 1: enable)

- INTF1: Interrupt request flag register [R/W], default value [0000]

INTF1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEF	IGBTOVF	SYNCF	INTF
Read/Write	R/W	R/W	R/W	R/W

INTF: INT external interrupt request flag. (0: inactive; 1: active)
SYNCF: SYNC external interrupt request flag. (0: inactive; 1: active)
IGBTOVF: IGBT over voltage active flag. (0: inactive; 1: active)
SURGEF: Surge active flag. (0: inactive; 1: active)

INTF with mask option for trigger type

INTS1 INTS0	Trigger type
00	Low active
01	Falling edge
10	Rising edge
11	Dual edge trigger

SYNCF with mask option for trigger type

SYNCS1 SYNCS0	Trigger type
00	High active
01	Rising edge
10	Falling edge
11	Dual edge trigger

If the interrupt request needs service, the programmer may set the corresponding INT enable bit to allow interrupt active. External interrupts are triggered by trigger type and set the related interrupt request flag (INTxF). The internal timer/counter interrupt is setting the TCPAF to 1, resulting from the timer/counter overflow. The time base interrupt TBxINT was provided 2 periodic interrupt request cycles for user operating a periodic routine.

When the corresponding interrupt enable and flag bits is set to 1, the CPU will active the interrupt service routine. Then CPU reads the service flag and check the request priority then

proceeds with the relative interrupt service. After CPU writes the corresponding bits to 0 in the INTxF register, the service flag will be cleared to 0(using STX #n, $m instruction). The INTF & INTF1 registers' bit can only write "0" to clear the flag. User writes "1" to Flag bit with no effect.

§ Peripheral function description:

1: System clock pre-scale

The system clock almost is the most high frequency of MCU. For various peripherals, application needs different clock source divided from system clock. TCPFS register is a selector for choosing suitable frequency (FS).

² TCPFS: System clock pre-scale register[R/W], default value [-000]

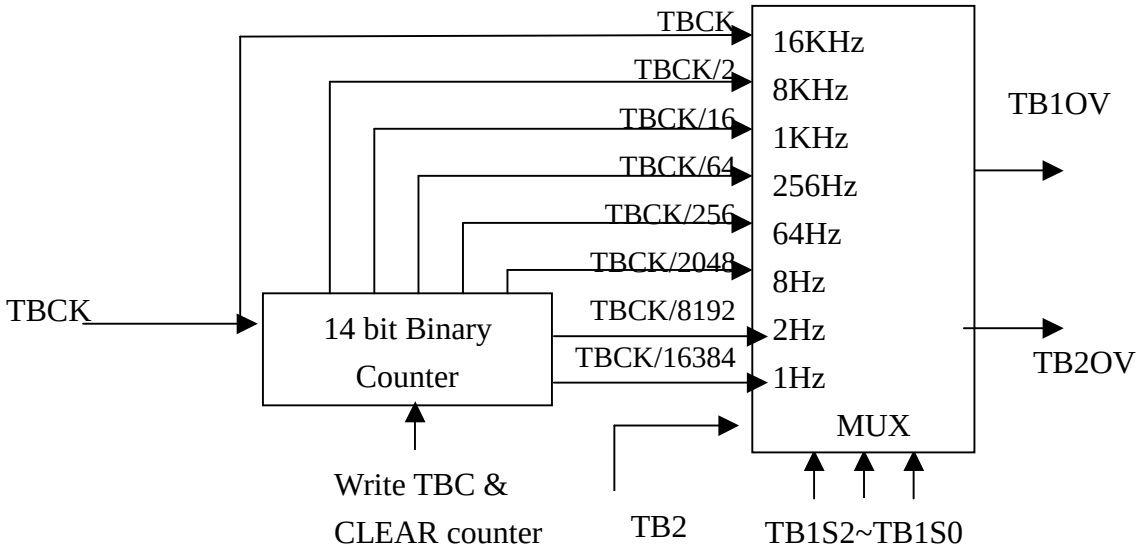
Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	FS2	FS1	FS0
Read/Write	-	R/W	R/W	R/W

FS2~FS0: the selector value of TCPFS register

FS2 ~ FS0	FS	FS2 ~ FS0	FS
0	OSCH/1	4	OSCH/16
1	OSCH/2	5	OSCH/32
2	OSCH/4	6	OSCH/64
3	OSCH/8	7	OSCH/128

2: Time Base Counter

The time base counter has 2 interrupt sources and both of them come from the peripheral internal RC oscillator or external RTC optioned by mask option. The time base 1st overflow output (TB1OV) can cause interrupt and the period is selected by TB1S2~TB1S0 in TBC register. The time base 2nd frequency (TB2OV) also offers two sample frequency options by TB2S bit in the TBC register.



² TBC: Time base control register[R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TB2S	TB1S2	TB1S1	TB1S0
Read/Write	R/W	R/W	R/W	R/W

TB1S2 ~ TB1S0: Base timer overflow frequency selection bits.

TB2S: Key sample source selection (0: 256Hz; 1:64Hz)

(Every time writing the TBCC will clear the time base counter)

TB2S	TB2OV
0	256Hz (TBCK/64)
1	64Hz (TBCK/256)

TBS2	TBS1	TBS0	**Base timer overflow frequency (TB1OV)**	32768HZ **TB1OV**
0	0	0	TBCK	16K HZ
0	0	1	TBCK/2	8K HZ
0	1	0	TBCK/16	1K HZ
0	1	1	TBCK/64	256 HZ
1	0	0	TBCK/256	64 HZ
1	0	1	TBCK/2048	8 HZ
1	1	0	TBCK/8192	2 HZ
1	1	1	TBCK/16384	1 HZ

- INTC0: Interrupt control register [R/W], default value [0000]

INTC0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESIE	TCPAIE	TB2IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

TB1IE: Enable time base 1st interrupt. (0: disable; 1: enable)

TB2IE: Enable time base 2nd interrupt. (0: disable; 1: enable)

- INTF0: Interrupt request flag register [R/W], default value [0000]

INTF0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESF	TCPAF	TB2F	TB1F
Read/Write	R/W	R/W	R/W	R/W

TB1F: Time base timer 1st interrupt request flag. (0: inactive; 1: active)

TB2F: Time base 2nd interrupt request flag. (0: inactive; 1: active)

3: 8 bits Timer/Counter/PFD (TCPA)

One 8-bits timer/counters/PFD (TCPA) with 4 kind clock sources and preload data buffer can implement as a timer or counter feature , PFD is programmable frequency divider can support sound /melody/carrier generator. The clock sources of TCPA are selected by TCPAS0 & TCPAS1 two bits of the timer control registers (TCPAC). TCPAOV is the timer or counter overflow signal and the rising edge will set the relative INT flag.

² TCPAC: Timer/counter/PFD control register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPALD	TCPAS1	TCPAS0	TCPAEN
Read/Write	R/W	R/W	R/W	R/W

TCPAEN: TCP counting enabled. (0: disable; 1: enable)

TCPALD: TCP auto-reload enabled. (0: disable; 1: enable)

TCPAS1 & TCPAS0: TCPA clock source selection bits.

TCPAS1	TCPAS0	**TCP A**
0	0	**FS**
0	1	**TCPA**
1	0	**TBCK**
1	1	**TB1OV**

FS: System scaled frequency.

TB1OV: Time base 1st overflow output.

TCPAOV: Timer/counter A′ overflow output.

TBCK: Peripheral clock source, 16KHZ.

TCPA: External input clock from pad shared with IO Port.

	PFD Output
TCP A	PFD

PFD: TCPA cycle time/2 output signal

- TCPADL: TCPA low nibble data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA3/TCPAD3	TCPA2/TCPAD2	TCPA1/TCPAD1	TCPA0/TCPAD0
Read/Write	R/W	R/W	R/W	R/W

TCPA3~TCPA0: reading the counter low nibble data.

TCPDA3~TCPAD0: writing TCPAD low nibble of data buffer.

- TCPADH: TCPA high nibble data register[R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPA7/TCPAD7	TCPA6/TCPAD6	TCPA5/TCPAD5	TCPA4/TCPAD4
Read/Write	R/W	R/W	R/W	R/W

TCPA7~TCPA4: reading the counter high nibble data.

TCPAD7~TCPAD4: writing TCPD high nibble of data buffer.

- TCPAD: Like a 8 bit TCP data register[R/W], default value [00H]

TCPAD	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Bit Name	TCPAD7	TCPAD6	TCPAD5	TCPAD4	TCPAD3	TCPAD2	TCPAD1	TCPAD0

The special R/W function for TCPA has different target, AS writing TCPAH/L registers that are updating preload data of the TCPAD. As read TCPAH/L registers that are the brand new TCPA counter value.

- INTC0: Interrupt control register [R/W], default value [0000]

INTC0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESIE	TCPAIE	TB2IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

TCPAIE: Enable interrupt of timer/counter A. (0: disable; 1: enable)

- INTF0: Interrupt request flag register [R/W], default value [0000]

INTF0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESF	TCPAF	TB2F	TB1F
Read/Write	R/W	R/W	R/W	R/W

TCPAF: Timer/counter A′ interrupt request flag. (0: inactive; 1: active)

.Timer

When TCPA works as a Timer, user needs give the preload data TCPAD for periodic interrupt. After initial setting, user starts the TCPA counting by setting TCPAEN=1, the TCPA cycle period is:

Tc = (selected clock cycle) * (TCPAD)

When user writes data to the TCPAD, the data just keep in TCPADL/H register. During the TCPAEN=1 command executed, the TCPAD 1's complement value will load into counter TCPA as initial value and start the timer function. Necessary TCPALD=1, timer run with reload feature as TCPA up counts and reaches the value 0f "FF_H" or 255. At the same time, interrupt request flag TCPAF will set activated, if software enables the corresponding interrupt enable bit, INT hardware will cause MCU interrupt service routine.

.PFD

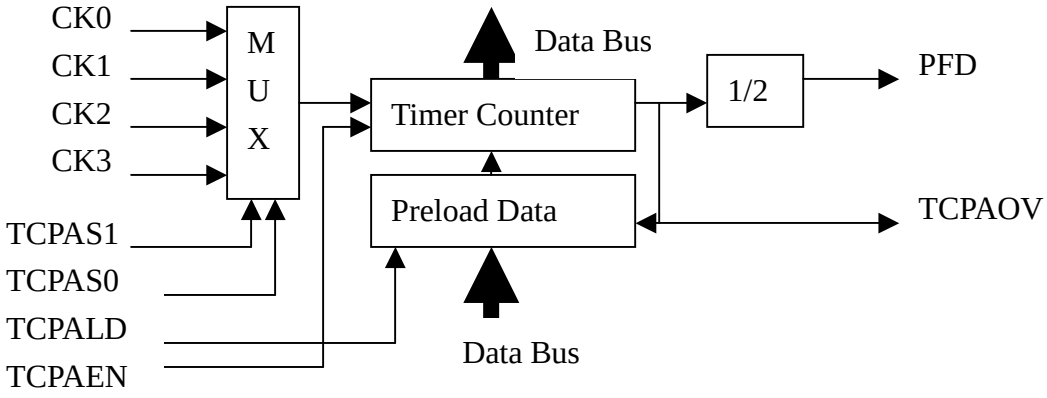
The PFD Mode includes in timer mode and the output frequency is:

PFD frequency = (selected clock frequency) / (2) / (TCPAD)

At this time, most users will disable the interrupt feature for tone or melody generation.

.Counter

Counter feature is implemented only by TCPALD=0, the TCPAD can be zero or not that depends on software needs. User starts & stops the counter by changing the TCPAEN bit value. On the save side, reading the counter value after stopping the count by disable TCPAEN=0, if reading the counter value during value changing that means clock in happening at the same time. The reading of counter value may disrupt for transient state. If 8 bit counter is not enough for counting, user can enable the interrupt and using the data RAM as software counter for extending the counter stage.

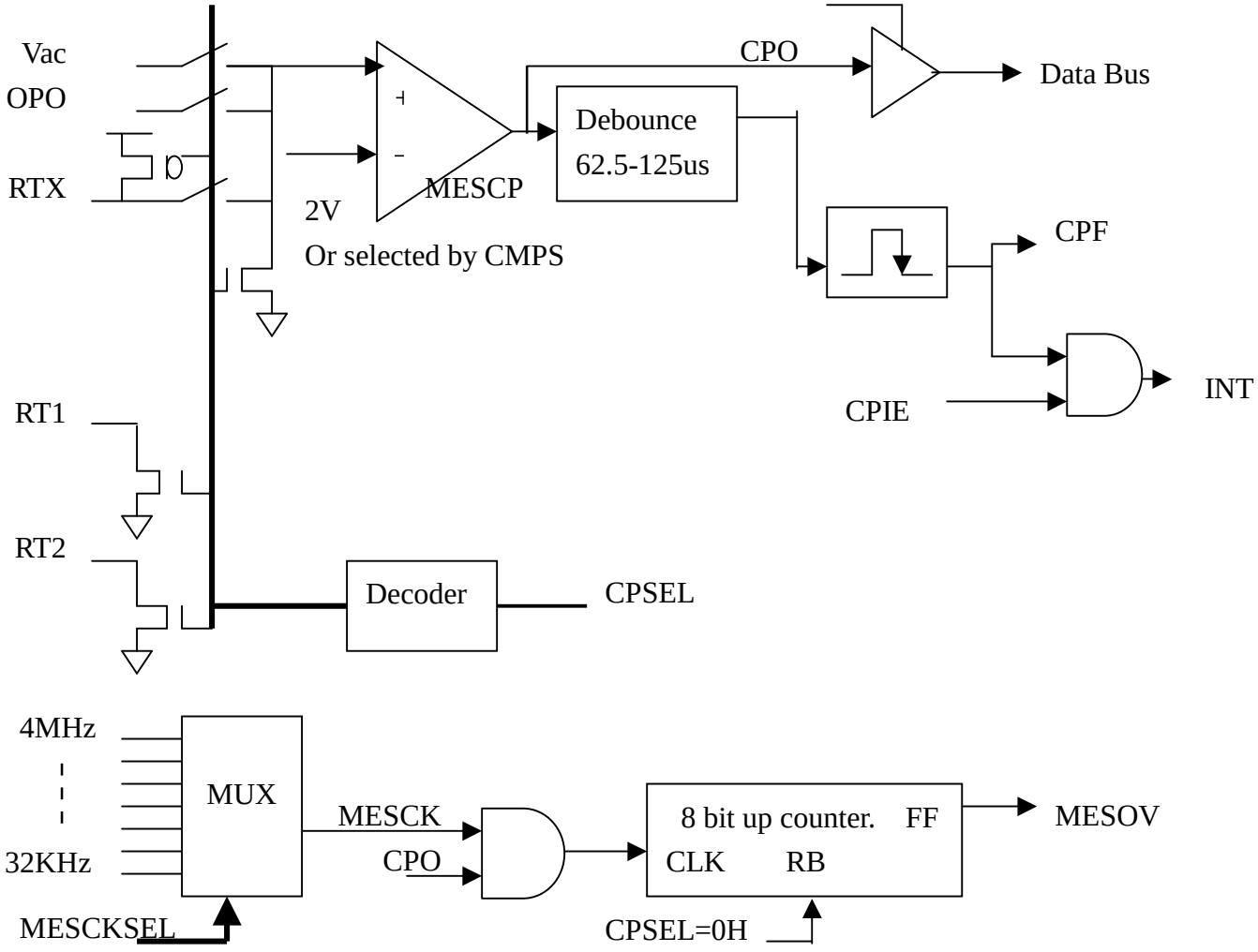


V1.0

Figure: Timer/Counter/PFD

4: Induction heating control

a. Common comparator and 8 bits counter for measuring:



One 8-bits counter (MES) with 8 kind clock sources can implement as a measuring meter feature, and a comparator (MESCP) can be arranged to support Voltage/ Current/ Thermal measuring. The clock sources of MES are selected by MESCKS0 & MESCKS1 & MESCKS2 three bits of the clock control registers (MESCKSEL). MESOV is the timer overflow signal and the rising edge will set the relative INT flag (MESF). To clear the MESF flag, user can write "0" or set CPSEL to "0". User write "1" to MESF flag bit with no effect.

The comparator (MESCP) with the channel selection register CPSEL can multiplex a channel once a time for measuring. No matter what channel selected, the comparator output signal CPO is always strobe, and filtered 100us to generate CPF through falling

edge detector. If CPF results to "active" and programmer set the interrupt request CPIE "enable", the CPU will active the interrupt service routine. The CPF registers' bit can write "0" to clear the flag. User writes "1" to flag bit with no effect. When CPSEL set to "0" or "F" also clear the CPF bit.

- MESCKSEL: Measuring clock of signal pulse width selection data register [R/W], default value [-000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	-	MESCKS2	MESCKS1	MESCKS0
Read/Write	-	R/W	R/W	R/W

MESCKS	MESCK	MESCKS	MESCK
000	4MHz	100	256KHz
001	2MHz	101	128KHz
010	1MHz	110	64KHz
011	512KHz	111	32KHz

- MESDL: Low nibble Measure data register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	MESD3	MESD2	MESD1	MESD0
Read/Write	R	R	R	R

- MESDH: High nibble Measure data register [R], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	MESD7	MESD6	MESD5	MESD4
Read/Write	R	R	R	R

MES data =128*MESD7+ 64*MESD6+ 32*MESD5+ 16*MESD4+ 8*MESD3+ 4*MESD2+ 2*MESD1+ MESD0

- INTC0: Interrupt control register [R/W], default value [0000]

INTC0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESIE	TCPAIE	TB2IE	TB1IE
Read/Write	R/W	R/W	R/W	R/W

MESIE: Enable interrupt of MES counter. (0: disable; 1: enable)

- INTF0: Interrupt request flag register [R/W], default value [0000]

INTF0	Bit3	Bit2	Bit1	Bit0
Bit Name	MESF	TCPAF	TB2F	TB1F
Read/Write	R/W	R/W	R/W	R/W

MESF: MES counter interrupt request flag. (0: inactive; 1: active)

² CPACK: Comparator acknowledge data register [R/W], default value [u-00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	CPO	SYNC	CPF	CPIE
Read/Write	R	R	R/W	R/W

CPIE: Enable interrupt of CPO falling-edge. (0: disable; 1: enable)

CPF: CPO falling-edge interrupt request flag. (0: inactive; 1: active)

CPO: Comparator data out signal.

SYNC: Magnetic coil synchronous signal

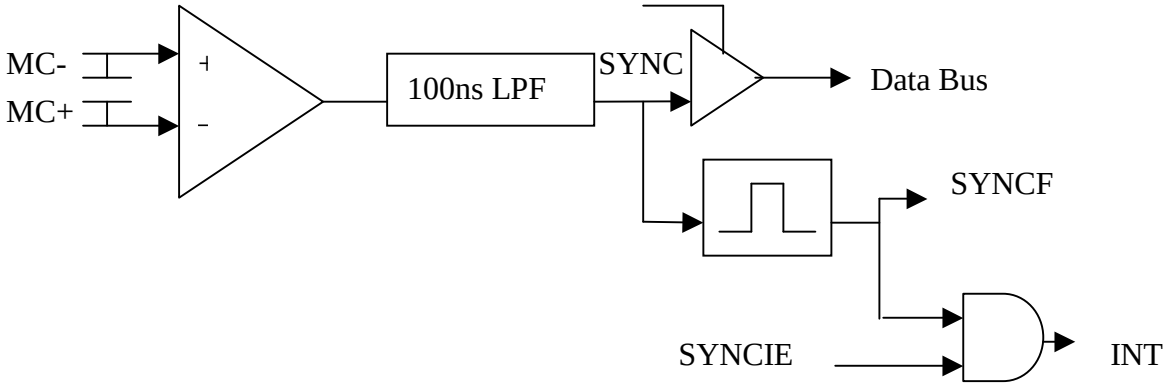
² CPSEL: Comparator channel Selection data register [R/W], default value [-000]

Register	Bit3	Bit2	Bit2	Bit0
Bit Name	-	CPSEL2	CPSEL1	CPSEL0
Read/Write	-	R/W	R/W	R/W

CPSEL	Operation	Discharge	Pull low	Counter
000	Clear	ON	ON	clear
001	Vac selected	OFF	OFF	Not clear
010	RT3 selected	OFF	OFF	Not clear
011	OPO selected	OFF	OFF	Not clear
100	RT1 selected	OFF	OFF	Not clear
101	RT2 selected	OFF	OFF	Not clear
110	Stop	OFF	ON	Not clear
111	Accumulate	ON	ON	Not clear

b. IGBT control:

1. Sync edge detector for PWM duty start, MC+ & MC- are come from Magnetic coil terminal.



² CPACK: Comparator acknowledge data register [R/W], default value [u-00]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	CPO	SYNC	CPF	CPIE
Read/Write	R	R	R/W	R/W

SYNC: Magnetic coil synchronous signal

² INTC1: Extended interrupt control register [R/W], default value [0000]

INTC1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEIE	IGBTOVIE	SYNCIE	INTIE
Read/Write	R/W	R/W	R/W	R/W

SYNCIE: SYNC interrupt request enable. (0: disable; 1: enable)

² INTF1: Interrupt request flag register [R/W], default value [0000]

INTF1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEF	IGBTOVF	SYNCF	INTF
Read/Write	R/W	R/W	R/W	R/W

SYNCF: SYNC external interrupt request flag. (0: inactive; 1: active)

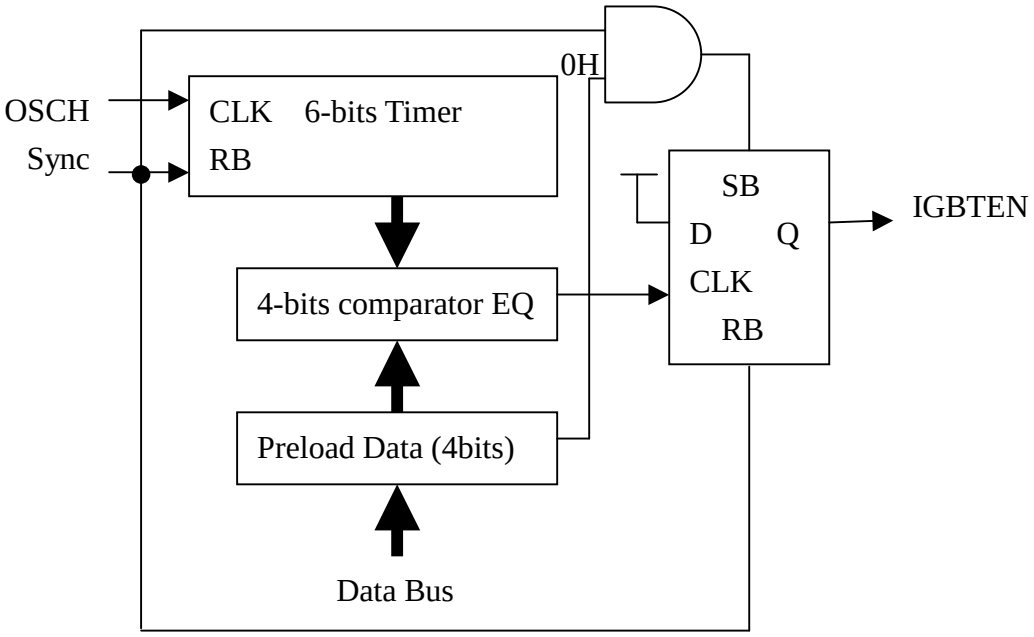
I

SYNCF with mask option for trigger type

SYNCS1 SYNCS0	Trigger type
00	High active
01	Rising edge
10	Falling edge

11	Dual edge trigger

2. Adjustable time for zero voltage turn-on



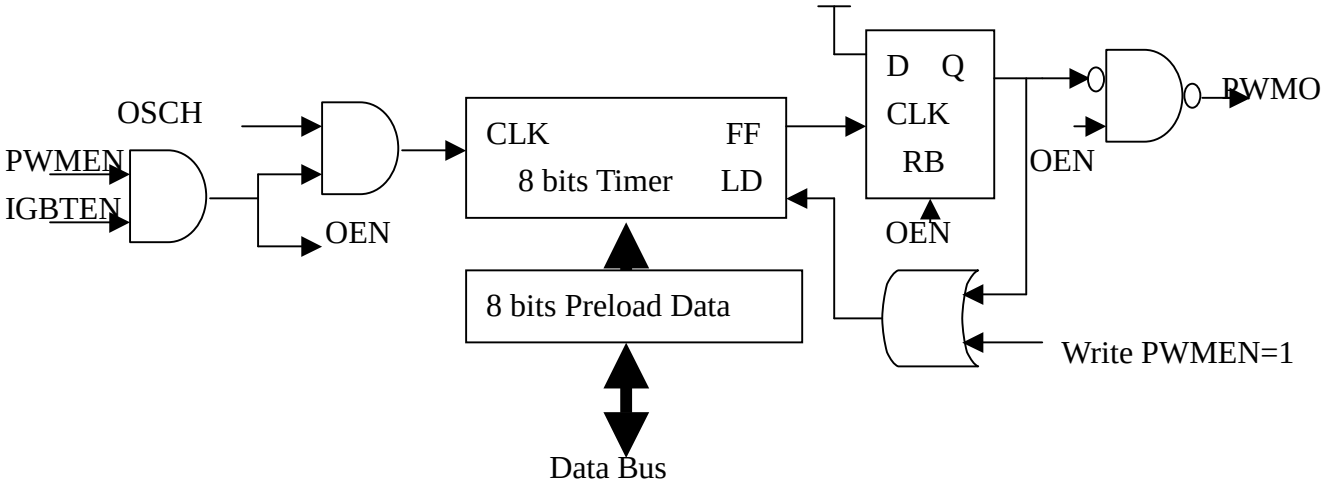
² TZERO: Adjustable time for zero voltage turn-on data register [R], default value [0000]

Register	Bit3	Bit2	BiT2	Bit0
Bit Name	TZERO3	TZERO2	TZERO1	TZERO0
Read/Write	R/W	R/W	R/W	R/W

TZERO data=8*TZERO3+4*TZERO2+2*TZERO1+TZERO0

TZERO time = (OSCH/4) * (TZERO)

3. 20~40KHz PWM duty control with target data



² PWMDL: Low nibble PWM data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWMD3	PWMD2	PWMD1	PWMD0
Read/Write	R/W	R/W	R/W	R/W

² PWMDH: High nibble PWM data register [R/W], default value [0000]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PWMD7	PWMD6	PWMD5	PWMD4
Read/Write	R/W	R/W	R/W	R/W

PWM data = 128*PWMD7 + 64*PWMD6 + 32*PWMD5 + 16*PWMD4 + 8*PWMD3 + 4*PWMD2 + 2*PWMD1+ PWMD0.

The PWM works as same as Timer, user needs give the preload data PWMDL/H for periodic operating. After initial setting, user starts the PWMO counting by setting PWMEN=1, the PWMO period is:

PWMO = (OSCH clock cycle)* (PWM) +TZERO time

When user writes data to the PWM, the data just keep in PWMDL/H register. During the PWMEN=1 command executed, the PWM 1's complement value will load into counter PWM as initial value and start the timer function. Necessary PWMEN=1, PWM run with reload feature as PWM up counts and reaches the value 0f "FF_H" or 255.

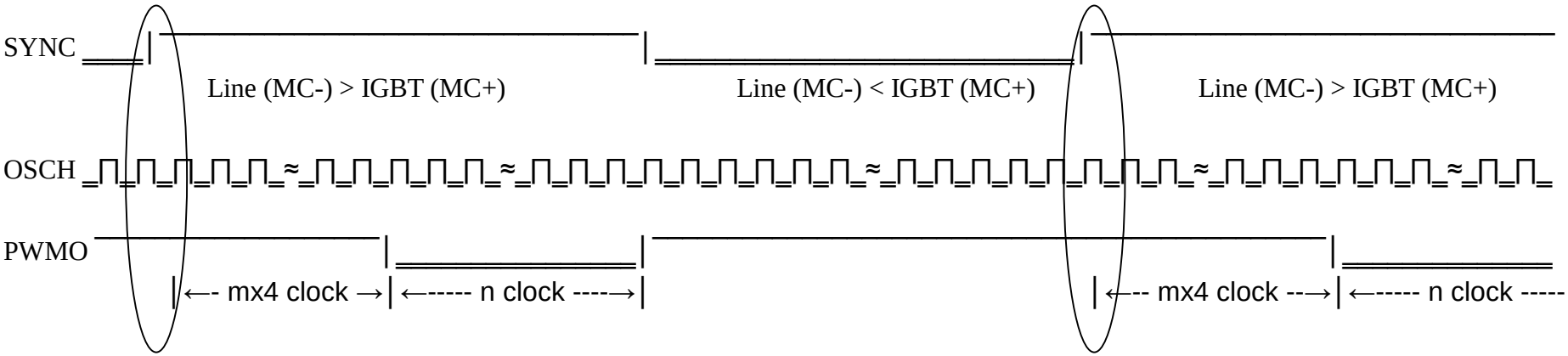
Programmer may keep in mind the IGBT control procedural:

I. IGBT off , if PWMEN=0 & IGBTEN=0

II. Wait TZEO counter runs, and if TZREO counter overflow then set IGBTEN=1.
III. PWM counter runs, and PWM counter reaches the target duty then IGBT off
IV. Wait SYNC signal transition
V. Go to I for next cycle

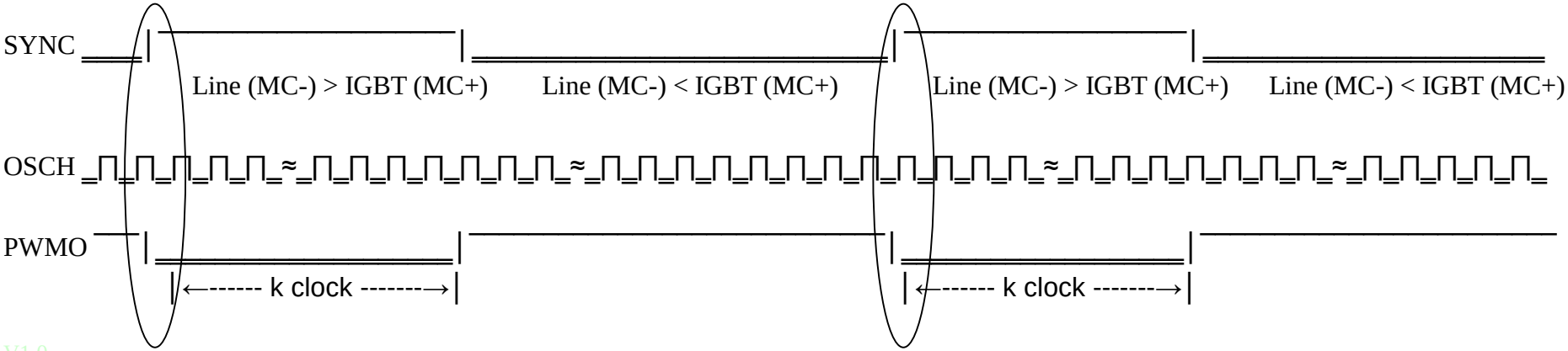
When PWMEN=1 & IGBTEN=1, the relationship between PWMO and SYNC has four kinds at different PWM duty with TZERO time. The timing diagrams are figured as follow:

i. SYNC Cycling: as TZERO=m (m≠0, m<16), PWM=n (n<256), OSCH=4MHz

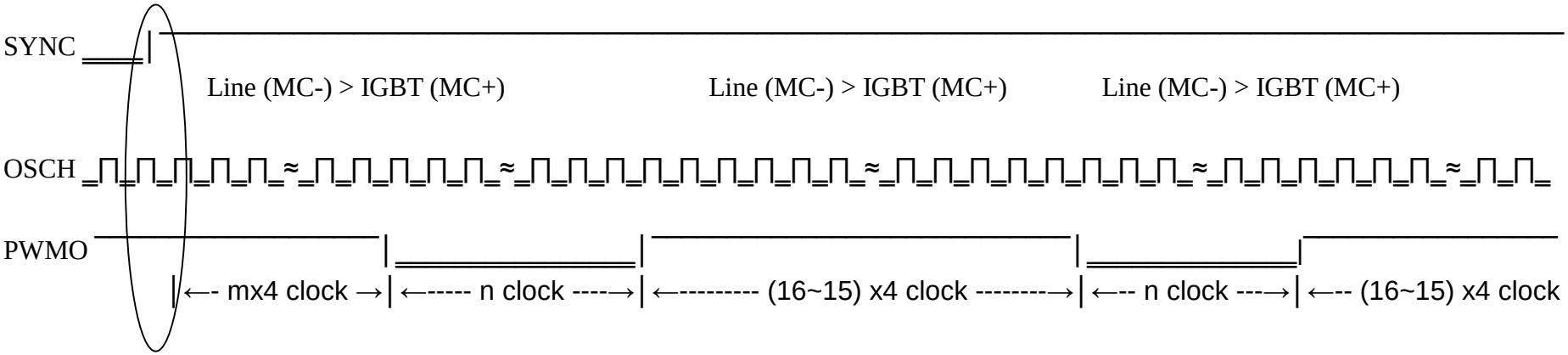


↑Asynchronous deviation

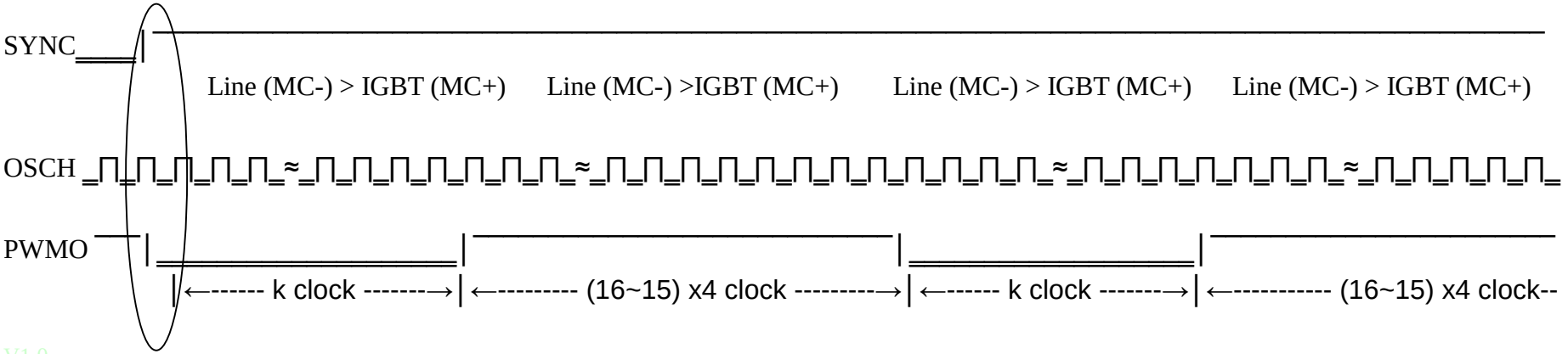
ii. SYNC Cycling: as TZERO=0, PWM =k (k<256), OSCH=4MHz

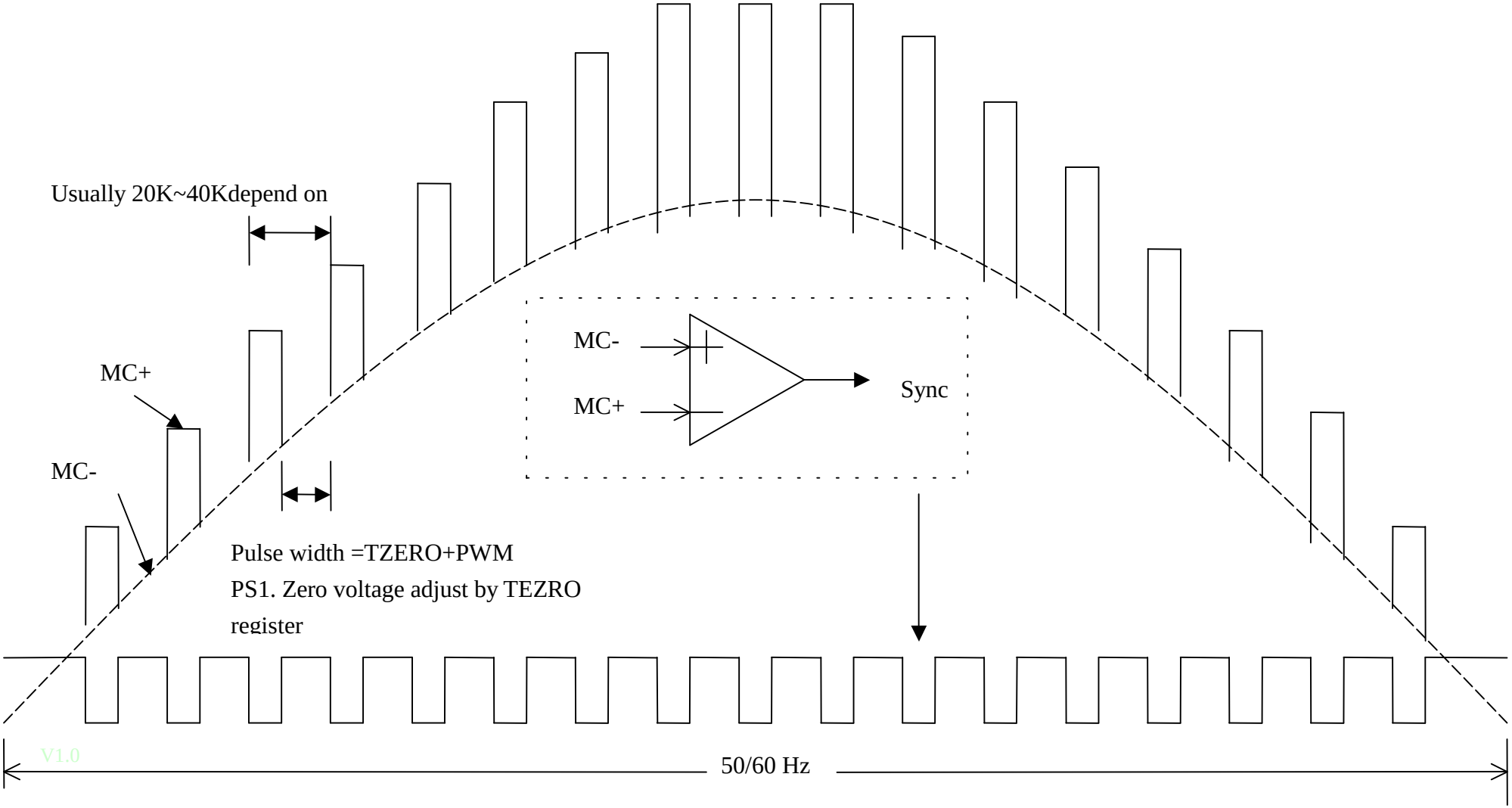


iii**. SYNC Not Cycling**: as TZERO=m (m≠0, m<16), PWM=n (n<256), OSCH=4MHz



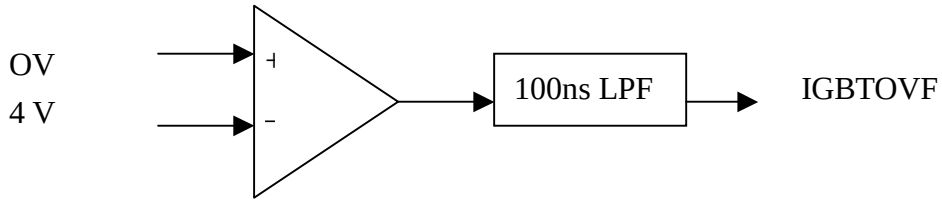
vi. SYNC Not Cycling: as TZERO=0, PWM =k (k<256), OSCH=4MHz



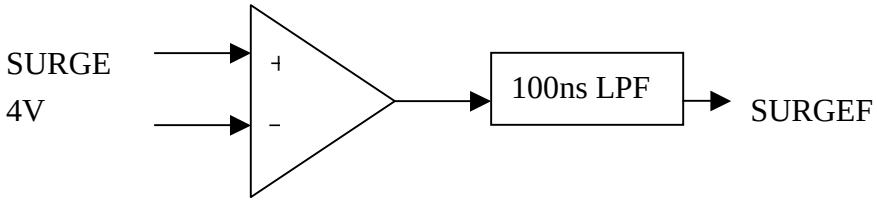


c. Over voltage protection:

1. IGBT Overshot voltage detection for slow down the power (start the warm up); STOP PWMO & set overshot flag



2. AC line voltage surge protection



IH interrupt (IGBTOV & Surge) works as warning request as the error conditions are detected. Any error condition happening, the hardware will STOP the PWM and stop the power. When IGBTOVF & SURGEF occurs, PWMEN automatically clears to be 0.

- INTC1: Extended interrupt control register [R/W], default value [0000]

INTC1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEIE	IGBTOVIE	INT1IE	INT0IE
Read/Write	R/W	R/W	R/W	R/W

IGBTOVIE: IGBT over voltage interrupt enable. (0: disable; 1: enable)

SURGEIE: Surge interrupt enable. (0: disable; 1: enable)

- INTF1: Interrupt request flag register [R/W], default value [0000]

INTF1	Bit3	Bit2	Bit1	Bit0
Bit Name	SURGEF	IGBTOVF	INT1F	INT0F
Read/Write	R/W	R/W	R/W	R/W

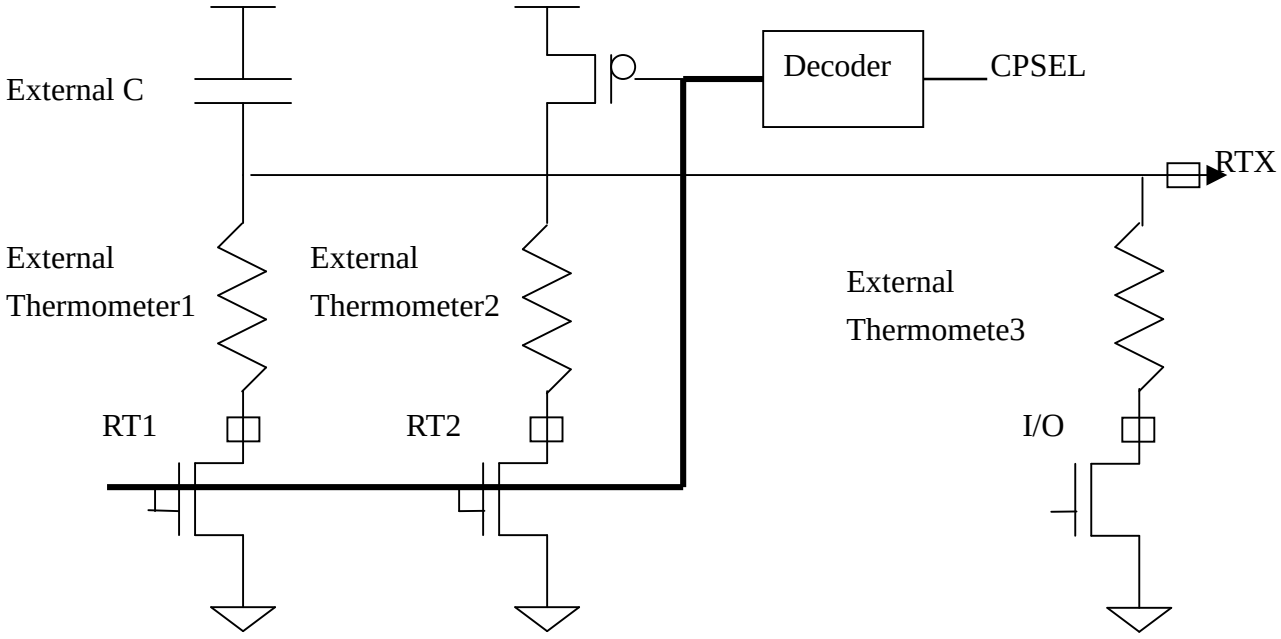
IGBTOVF: IGBT over voltage active flag. (0: inactive; 1: active)

SURGEF: Surge active flag. (0: inactive; 1: active)

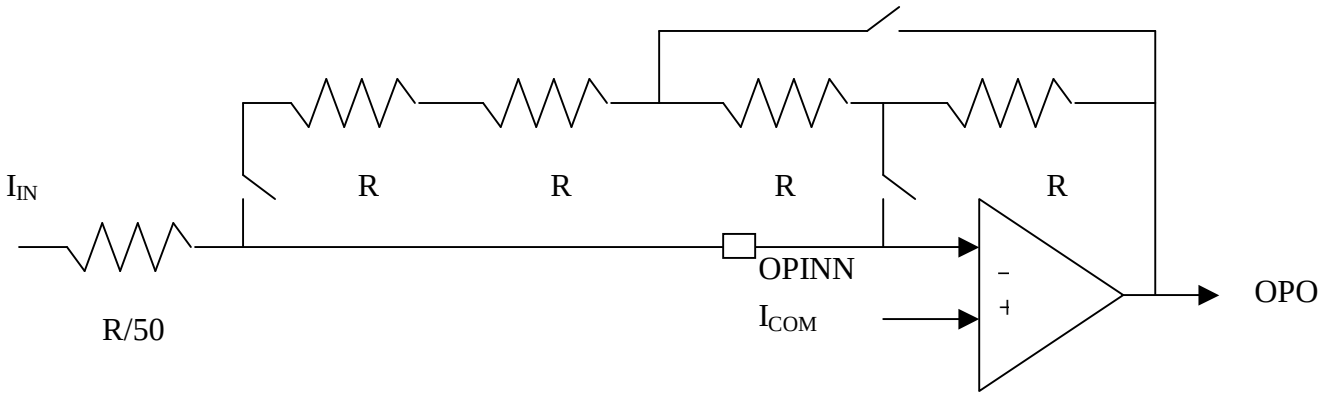
d. Thermal resistor condition check by counts

In the measurement application, a resistor type sensor can rely on this kind RC network to convert the various resistance value as relative different counter that uses as the same clock source of counter. First all, the external C was discharged to VDD while CPSEL set the appropriate value as 111 or 000. Then, select a thermometer channel (RT1 or RT2) to measure the charge time by the common comparator and 8 bits counter.

The resister of RC network is the main role to measure temperature. User can configure I/O pin as open drain to select which resister will act as the role. And select RT1 or RT2 which is as the common channel for measuring. The application is as follow:



e. OP Amp gain factor



² OPGFSEL: OP AMP Gain Factor selection register [R/W], default value [--00]

OPGFSEL	Bit3	Bit2	Bit1	Bit0
Bit Name	CMPS1	CMPS0	OPGFS1	OPGFS0
Read/Write	R/W	R/W	R/W	R/W

OPGFS[1:0]	Gain
00	25
01	50
10	100
11	200

CMPS[1:0]	Comparator Voltage Level
00	0.5V
01	1.0V
10	2.0V
11	3.0V

5: IO Pad Cells

The main features of pad cell are including ESD/EFT protection and general I/O access. A general I/O pad cell can be configured as input with or without pull-up resistor, or working as a CMOS or NMOS output driver. The input pad cell must have pull-up resistor for avoiding a floating state when user doesn't care or not be used. For concerning the standby current, user can use data register or I/O control register to fit the application.

. I/O File Register

² PAC: Port A I/O control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PAC3	PAC2	PAC1	PAC0
Read/Write	R/W	R/W	R/W	R/W

PAC3~PAC0: port A′ I/O control register.

² PA: Port A data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PA3	PA2	PA1	PA0
Read/Write	R/W	R/W	R/W	R/W

PA3~PA0: port A′ data register.

² PBC: Port B I/O control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PBC3	PBC2	PBC1	PBC0
Read/Write	R/W	R/W	R/W	R/W

PBC7~PBC0: port B I/O control register.

² PB: Port B data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PB3	PB2	PB1	PB0
Read/Write	R/W	R/W	R/W	R/W

PB3~PB0: port B data register.

- PCC: Port C I/O control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PCC3	PCC2	PCC1	PCC0
Read/Write	R/W	R/W	R/W	R/W

PCC3~PCC0: port C I/O control register.

- PC: Port C data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PC3	PC2	PC1	PC0
Read/Write	R/W	R/W	R/W	R/W

PC3~PC0: port C data register.

- PDC: Port D I/O control register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PDC3	PDC2	PDC1	PDC0
Read/Write	R/W	R/W	R/W	R/W

PDC3~PDC0: port D I/O control register.

- PD: Port D data register [R/W], default value [1111]

Register	Bit3	Bit2	Bit1	Bit0
Bit Name	PD3	PD2	PD1	PD0
Read/Write	R/W	R/W	R/W	R/W

PD3~PD0: port D data register.

.I/O PAD Cell Structure & Function Description

.. IO Port with external input

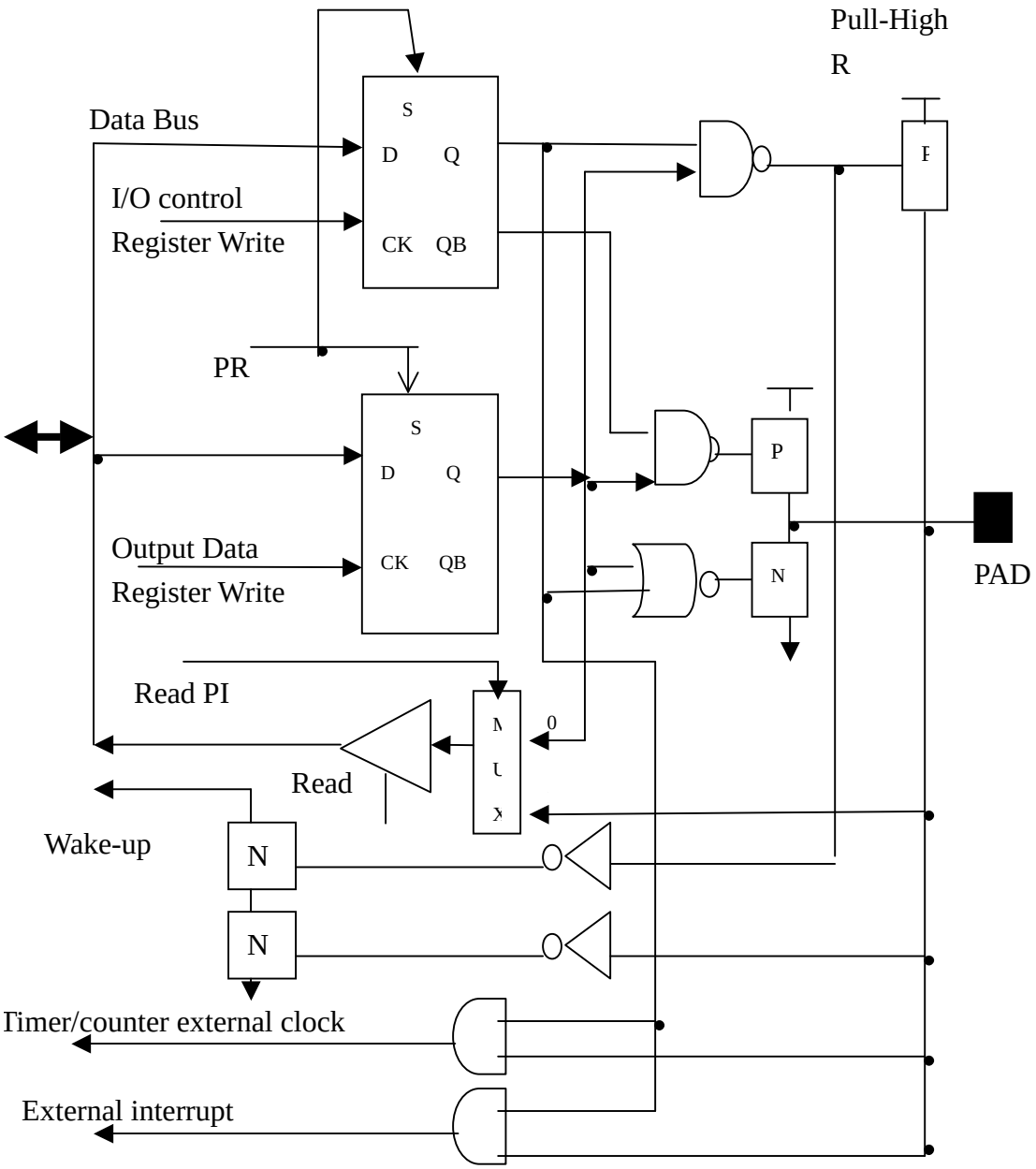
The input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application. An additional feature supports the interrupt input triggers and Timer external clock sources.

I/O control Data	Output data	Pull-up R	Wake-up feature	External inputs
0	X	No	No	No
1	0	No	No	Enable
1	1	Enable	Enable	Enable

X: don't care the value

I/O control Data	MODE	PAD
0	Output mode	Output Register data Q
1	Input mode	Input data

Read PI	Read Input Data
0	Output Register data Q
1	PAD input data



ure IO-A: Standard IO Port with wake-up/interrupt/timer clock inputs

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I/O port with internal output

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. If enable internal output by mask option, the internal output will control by output data (on/off) and outputs to PAD.

I/O control Data	Output data	Pull-up	Wake-up
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value

I/O control Data	Internal output	PAD
0	enable	Output Register data Q*internal data
0	disable	Output Register data
1	X	PAD input data

X: don't care the value

Read PI	Mode	Read Input Data
0	Output mode	Output Register data Q
1	Input mode	PAD input data

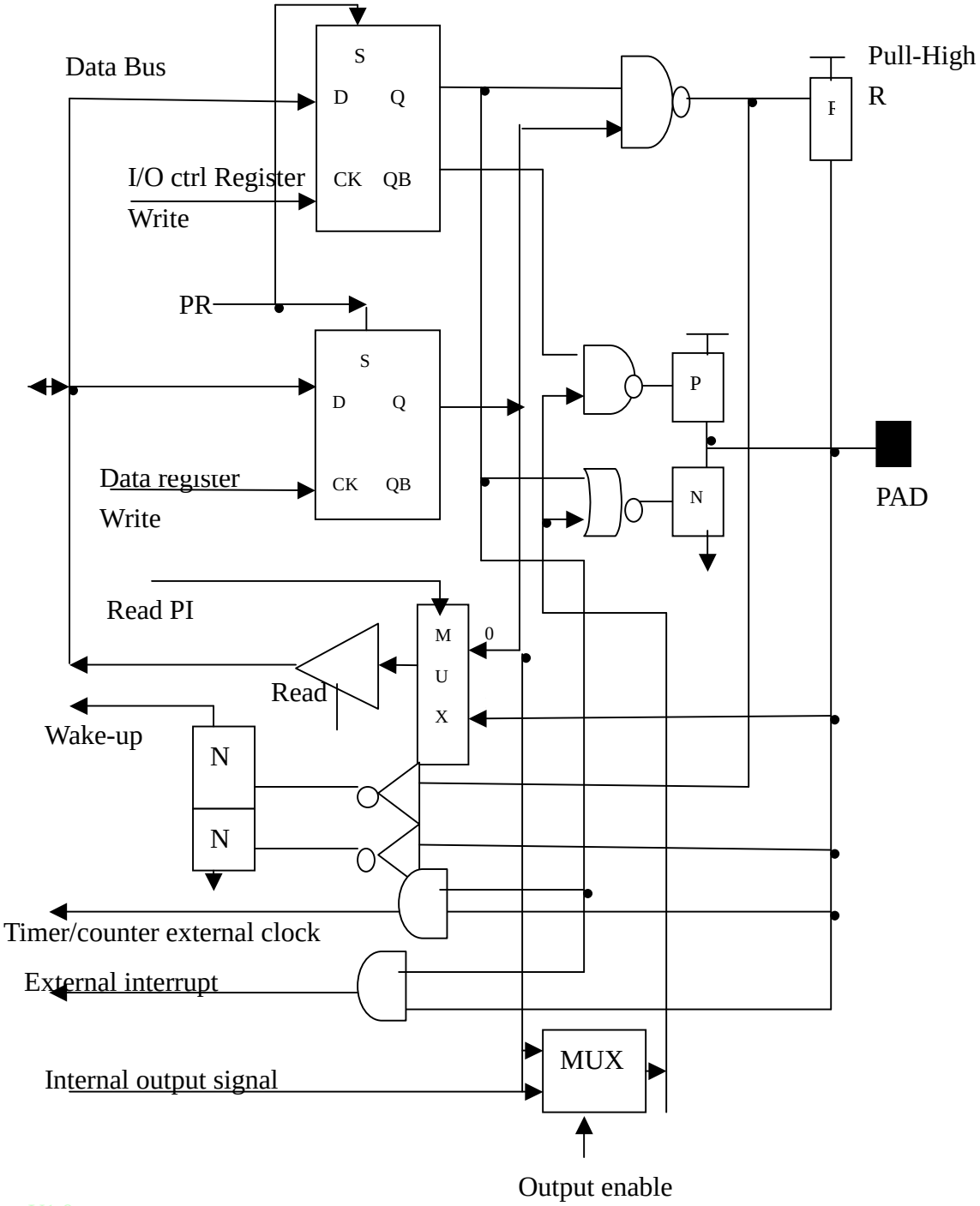


Figure IO-B: Standard I/O Port with internal output signal

Standard IO Port

The standard input/output port has the I/O control register for switching input or output mode and output data register stores the output data in output mode. If control register=1 and output data=1, the I/O port is programmed as input with pull-up resister and also actives the wake-up function. User intends to read the port data with differed read instruction. The read PI is reading data comes from PAD input data. The data register reading result will have the same value with output register data. Software can performs a configuration (data=0, changing the control 0 or 1) for open drain type that specifies suitable for key scan application.

I/O control Data	Output data	Pull-up	Wake-up
0	X	No	No
1	0	No	No
1	1	Enable	Enable

X: don't care the value

I/O control Data	MODE	PAD
0	Output mode	Output Register data Q
1	Input mode	Input data

Read PI	Read Input Data
0	Output Register data Q
1	PAD input data

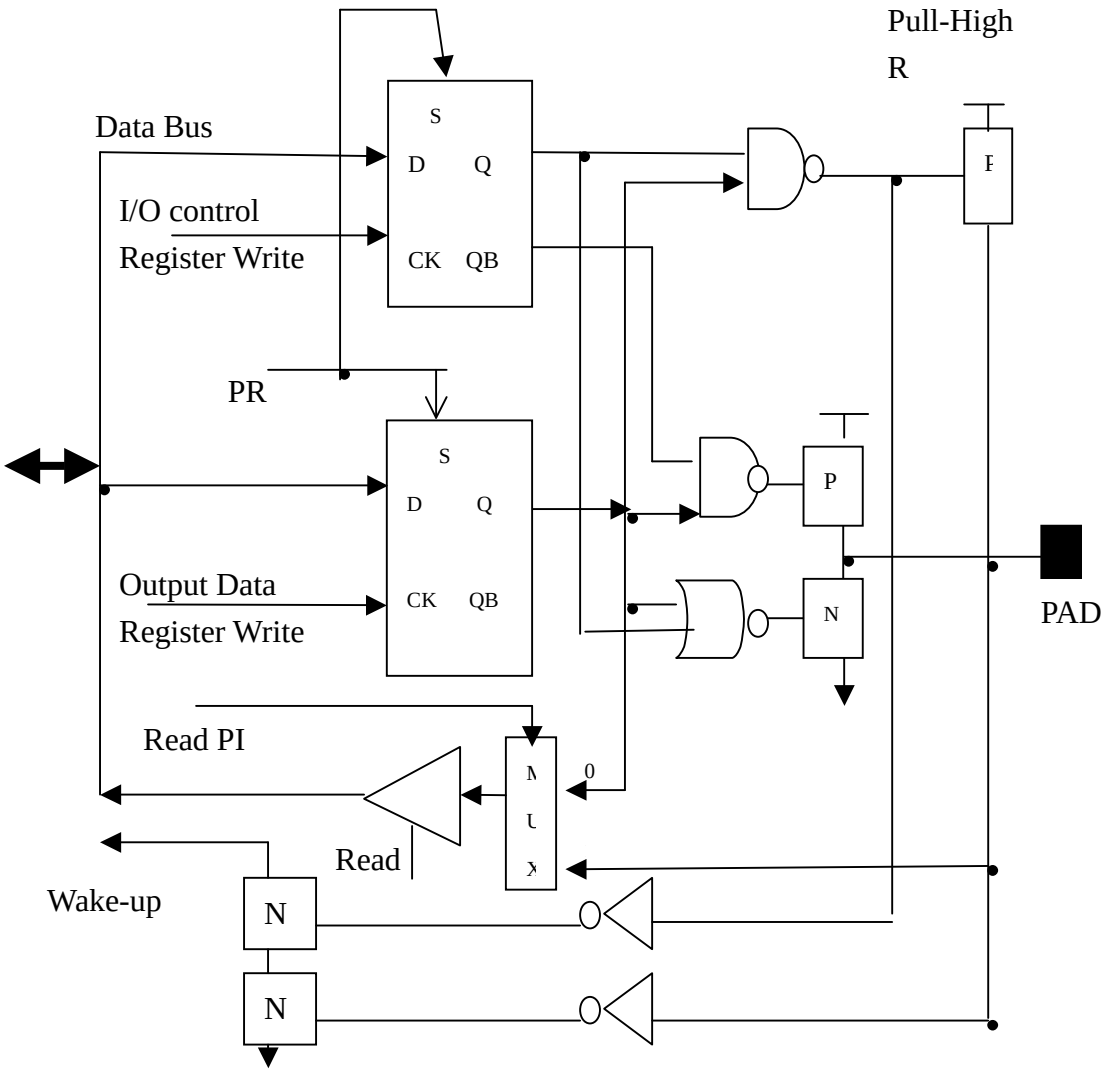


Figure IO-C: Standard IO Port

§ Mask Option Table:

All the OTP mask option register can open for user to reset the initial value, but should enable the MRO. User writes MRO address first then changes the target mask option register data. The MRO enable will be cleared with other writing address.

² MOP1: external INT type option register [R/W], default value [0000]

Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	SYNCS 1	SYNCS0	INTS1	INTS0
Read/Write	R/W	R/W	R/W	R/W

² MOP2: PFDB enable register [R/W], default value [0000]

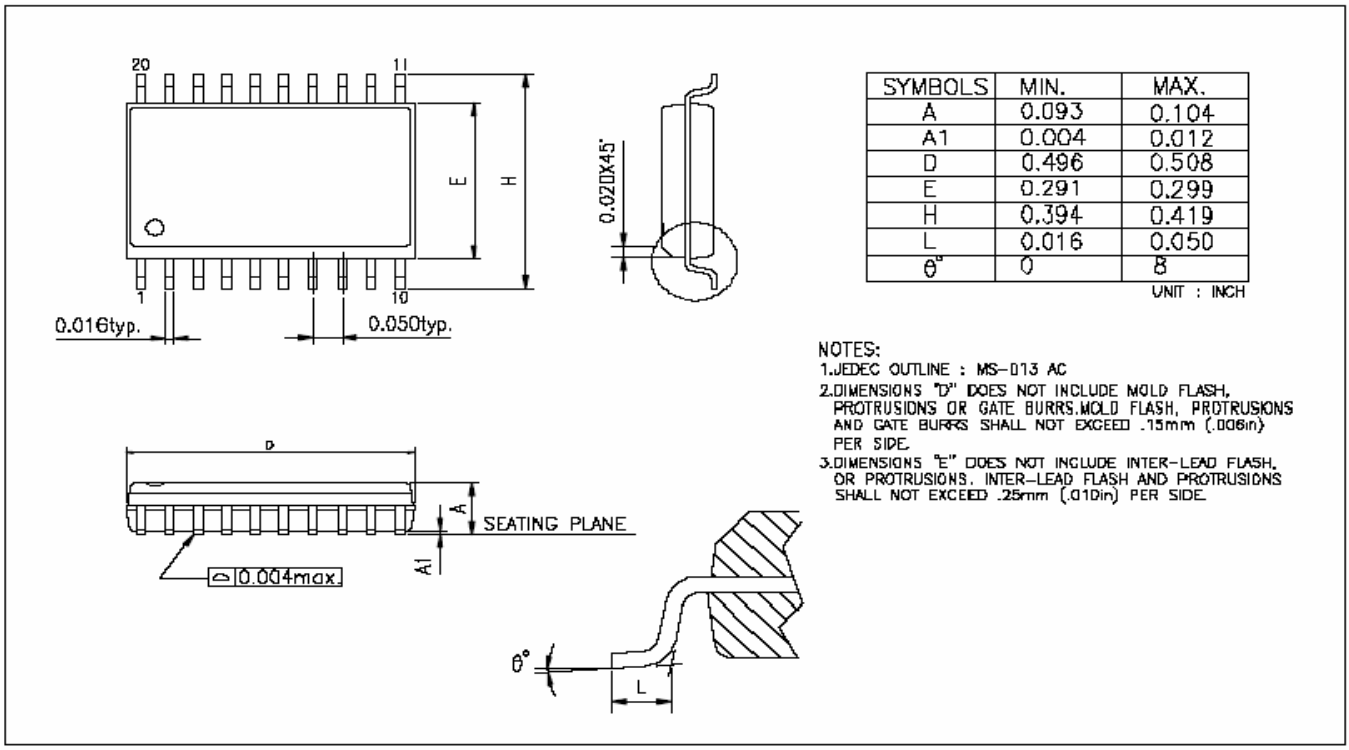
Mask option	Bit3	Bit2	Bit1	Bit0
Bit Name	-	-	-	PFDB
Read/Write	-	-	-	R/W

The following table shows the mask option in this chip. All the mask options must be defined clearly and ensure to meet user's proper function.

No.	Mask Option	Function Descriptions	
+2	SYNCF trigger type SYNCS1,SYNCS0	00	High level trigger
		01	Rising edge trigger
		10	Falling edge trigger
		11	Dual edge trigger
+2	INTF trigger type INTS1,INTS0	00	Low level trigger
		01	Falling edge trigger
		10	Rising edge trigger
		11	Dual edge trigger
+1	PFDB	0	PFDB output disable
		1	PFDB output enable

§ Package & PAD Information:

20-SOP

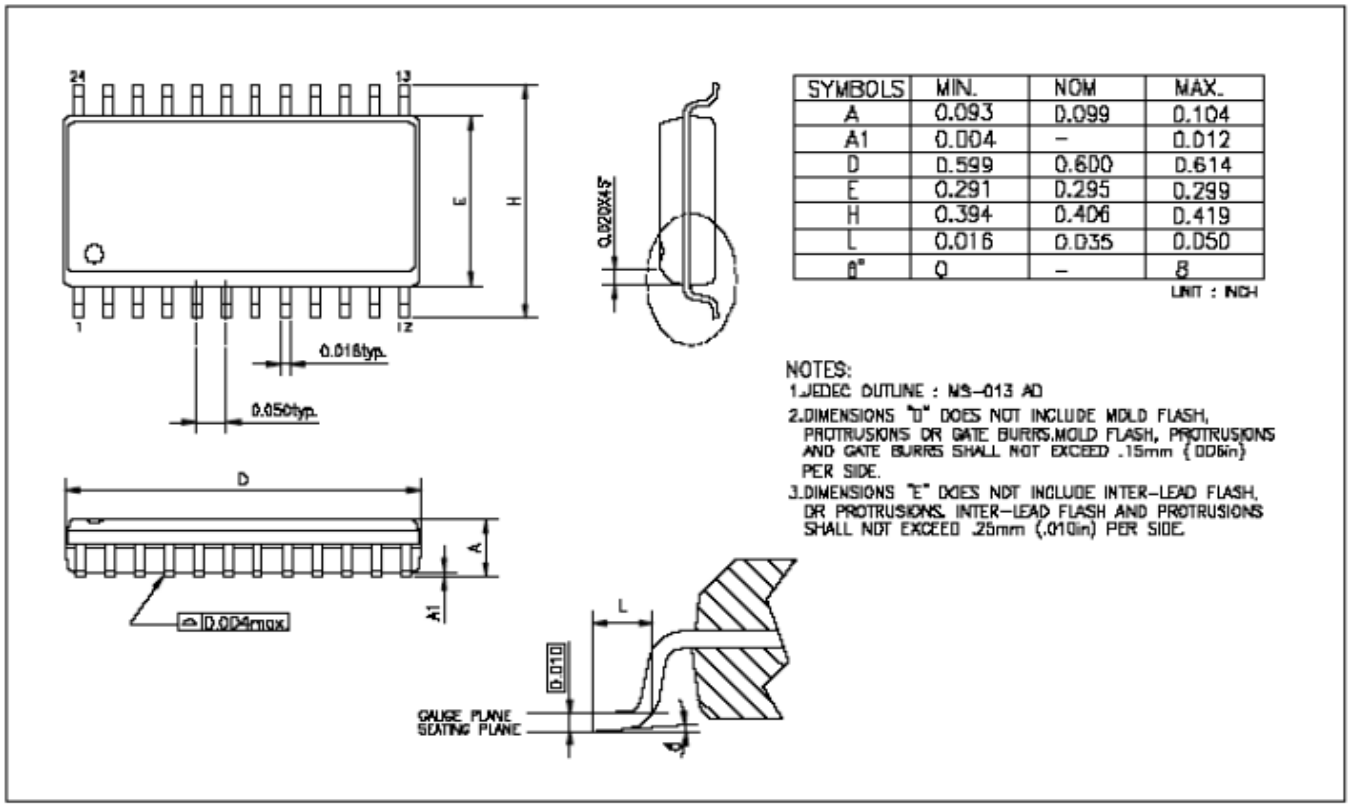


SYMBOLS	MIN.	MAX.
A	0.093	0.104
A1	0.004	0.012
D	0.496	0.508
E	0.291	0.299
H	0.394	0.419
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-013 AC
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.01Din) PER SIDE.

24-SOP

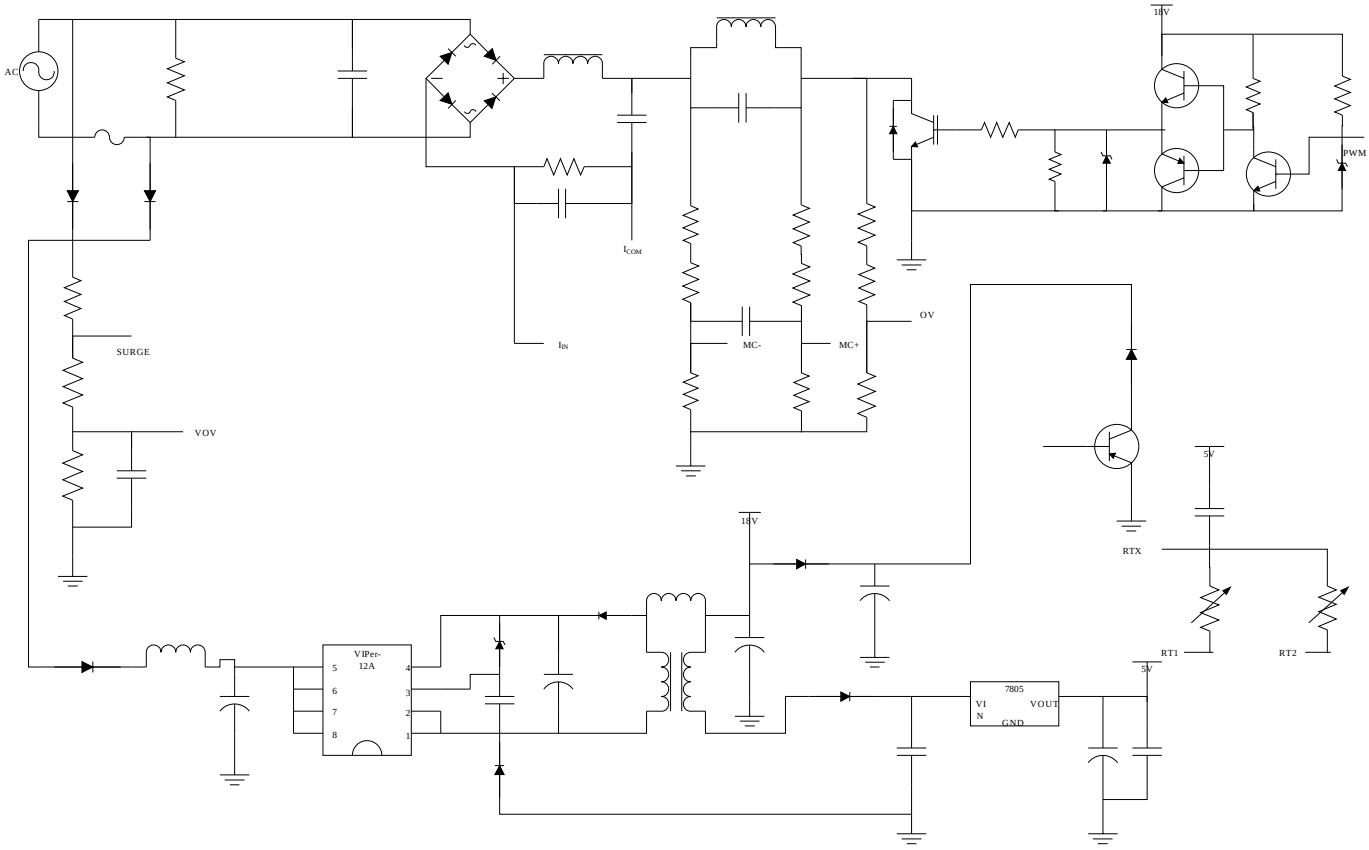


SYMBOLS	MIN.	NOM	MAX.
A	0.093	0.099	0.104
A1	0.004	–	0.012
D	0.599	0.600	0.614
E	0.291	0.295	0.299
H	0.394	0.406	0.419
L	0.016	0.035	0.050
θ°	0	–	8

UNIT : INCH

§ Application Circuit:

Preliminary



§ Ordering Form:

Preliminary

a. Package form : TTU(R)03A-zzz
b. Chip form : TCU(R)03A-zzz
c. Wafer base : TDU(R)03A-zzz

Modified Record:

Date	Name	Version	Page	Content
2007/4/27	Hans Yang	V0.0-000	1-41	Preliminary
2007/7/10	Hans Yang	V0.0-001	2	Add IH functional description
			5	Add IH Block Diagram
			11	Cancel CPU machine cycle
			14	Add LVNCR functional description
			26	Add TZERO time calculation
			24,28	Fix typing mistake
2007/7/25	Jason Lin	V0.0-001	10	Add CLRWDT address
			12	Modify Clear WDT method
2007/8/14	Hans Yang	V0.0-002	1	4K ROM
			6	PWMO NMOS open drain
			10,31	Add OPGFSEL address
			23	De-bounce replace low pass filter

2007/8/20	Hans Yang	V1.0-000	3,4	Modify Package
			5	Modify IH Block
			6	Modify Pin description
			8	Modify Memory map
			10,12	Modify Clear WDT method
			10,28	Cancel PINF
			23	Clear MESF & CPF by CPSEL
			25	Add reading Sync
			26	Modify TZERO block
			31	Modify OPGFSEL block
2007/8/22	Jason Lin	V1.0-000	7	ESD > 5 KV
			7	Minimum operating voltage
			8	System stable time after power up :1ms
			31	CMP voltage level selection 1/2/3/4 V
2007/9/6	Hans Yang	V1.0-000	1	4-Stack
			6	Add I_{OUT}, OPO, RTX pin. Change RT1, RT2 pin type

			23	Modify MESCP negative voltage input
			25	Add CPSEL=0011 for IOPO
			31	Change thermal resistor measure diagram
			32	Modify CMP voltage selection
			27,28,29	Add PWMO & SYNC timing diagram
2007/9/7	Hans Yang	V1.0-000	6	Add RI_{OUT}
			23	Modify MESCP channel selection block
			25	Modify CPSEL
			31	Change thermal resistor measure diagram
2007/9/10	Hans Yang	V1.0-000	5	Modify IH Block
			31	Cancel IO thermal resistor selection
2007/9/27	Hans Yang	V1.0-000	2,3	Change Package type
			5	Modify IH Block
			6	Add I_{COM}
2007/10/09	Y.B.C	V1.0-000	2,3	Change Package type
2007/11/2	Hans Yang	V1.0-000	12-15	LVREN stuck at "1"

2007/11/14	Hans Yang	V1.0-000	8	Change OST to 64ms
			13,14	Cancel CPU reset & define System Reset.
			32	Modify Comparator level for OP AMP
2007/11/21	Hans Yang	V1.0-000	30	Expand IHF to IGBTOVF & SURGEF
2007/11/30	Hans Yang	V1.0-000	29	Modify SYNC not Cycling timing diagram
2007/12/24	Y.B.C	V1.0-000	3	Modify 24-pin & 30-pin Package type
2007/12/28	Hans Yang	V1.0-000	6,39,40	Add STD I/O description
2005/4/21	Hans Yang	V1.0-000	30	Add Sync V.S. PWM waveform
2008/5/5	Hans Yang	V1.0-000	2,3,6	Add OPINN pin
			5,25,32	Change RI_{OUT} to RT3
2008/5/19	Hans Yang	V1.0-000	15,16,25,26	Change INT1 to SYNC interrupt
2008/5/21	Hans Yang	V1.0-000	16,26,43	Change SYNCF property
2008/8/7	Hans Tang	V2.0-000	2,3	Add Package type 20 SOP-B
2008/9/17	Hans Tang	V2.0-001	2,3	Add Package type 20 SOP-C